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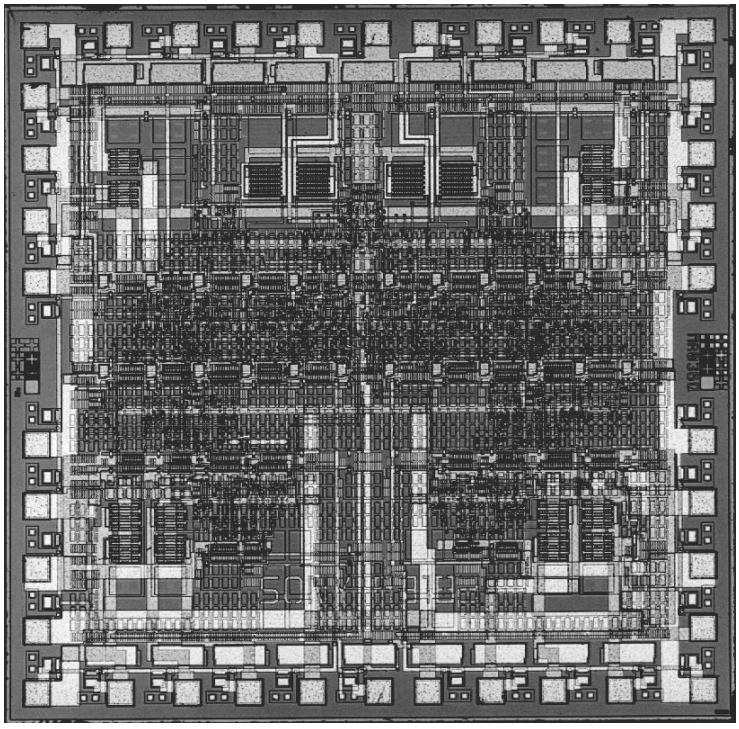
ATLAS Thin Gap Chamber

Amplifier-Shaper-Discriminator ICs and ASD Boards



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1 Introduction

The Thin Gap Chambers (TGCs) [1,2] dedicated for the forward muon Level-1 trigger must provide fast information on muon tracks traversing the TGCs in an environment of high background hits. Wires and strips are read out in binary mode to identify muon trajectories. The anode wires of the TGCs are arranged in the azimuthal direction and provide the radial measurement, while readout strips orthogonal to these wires provide the azimuthal measurement. Several wires are ganged together, where the number of the ganged wires depends on the desired granularity. Both wire and strip signals are used for the muon trigger [3,4].

The TGC system must provides information that enables:

- discrimination on muon transverse momentum, p_T, in the Level-1 trigger
- bunch-crossing identification
- fast and coarse track information for the higher-level triggers
- second coordinate measurement in the non-bending projection with a resolution of approximately 10^{-3} radians

These requirements define the condition on both the time resolution (less than the bunch-crossing interval) and the spatial resolution of the TGC. The TGC system indeed fulfills the requirements, since the intrinsic time jitter of the chamber is less than 25ns and fine granularity is easily attained by using anode signals.

The requirements on the Amplifier-Shaper-Discriminator (ASD) IC and the ASD Board for the TGC, besides low cost and low power consumption, are the following:

- fast discriminated signal with small time jitter
- stable operation for up to 100 kHz input signal rate per channel
- high reliability in the ATLAS cavern for ten or more years

The first requirement means fast signal processing with a low noise. However, the TGC has large detector capacitance that contradicts with the requirement for low noise and fast signal processing. Hence an appropriate technology choice and optimization of the circuit are essential. The event rate of 100kHz can be achieved without much difficulty. The last requirement demands radiation tolerant electronics that can survive 130Gy dose and $1.2\times10^{12}/\mathrm{cm}^2$ of 1MeV-equivalent-neutron fluence.

As a summary, the TGC ASD must have a good time resolution for bunch-crossing identification and a high rate capability to cope with high background hits, and must be robust against irradiation for the longtime operation.

2 Basic detector signal characteristics and their modeling

Both of the wire signals and the strip signals are used for the Level-1 muon trigger. Figure 2-1 shows an electrical model (cross-sectional view) of a TGC doublet where two TGCs are mounted on both side of a paper honeycomb core. Parameters of the model are summarized in Table 2-1.

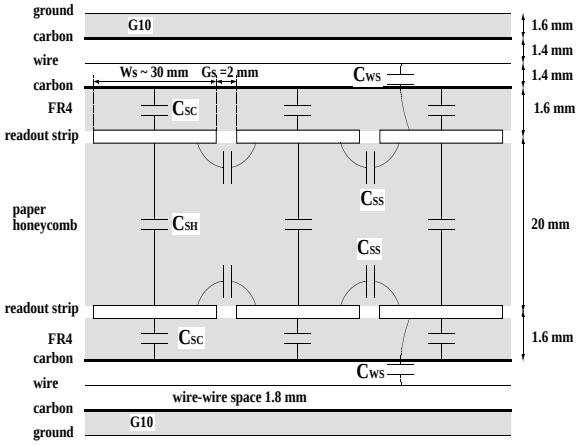

Figure 2-1 Electrical model of a TGC doublet.

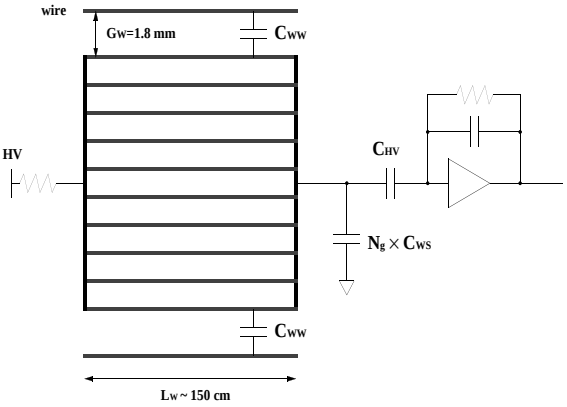

Figure 2-2 Electrical model of the wires.

Table 2-1 Parameters of an electrical model for the TGC doublet

TGC geometry	
# of wires to be ganged together	N_g = 5 ~ 32
wire length	L_W = 0.5 ~ 1.7 m
strip length	L_S = 1.2 ~ 2.3 m
wire-wire space	G_W = 1.8 mm
inter-strip gap	G_S = 2.0 mm
wire-carbon gap	G_{WC} = 1.4 mm
carbon plane - strip gap	G_{CS} = 1.6 mm
strip width	W_S = 15 ~ 53 mm
HV blocking capacitance	C_{HV} = 235 pF
Resistance values	
carbon plane	ρ = 1MΩ / square
wire	R_W = 30 Ω / m
between strips	$R_{SS} = \rho \cdot G_S / L_S$ = 2 kΩ (G_S = 2.0 mm, L_S = 1 m)
Capacitance values between:	
wire to strip, via carbon plane	C_{WS} = 11 pF / m / wire, 0.31 pF / cm^2 / strip
two wires	C_{WW} = 6.5 pF / m
strip and carbon plane	C_{SC} = 2.94 pF / cm^2
strip-to-strip via honeycomb	C_{SH} = 0.055 pF / cm^2
strip-to-strip in same chamber	C_{SS} = 20 pF / m
Detector capacitance (C_D)	
C_{WG}(wire group capacitance)	$C_{WG} = Ng \times C_{WS} + 2\ C_{WW}$ = 123 pF / m (Ng=10)
C_D (wire-group)	$C_D = C_{WG} \times C_{HV} / (C_{WG}+C_{HV})$
C_S (strip)	$C_S = L_S \times W_S \times (C_{WS}+C_{SH}) + C_{SS}$ = 129.5 pF / m (W_S=30mm)
C_D (strip)	$C_D = C_S$

Figure 2-1 shows the anode signal path. Several wires (the number depends on the desired granularity at that η value) are ganged together to provide an anode signal. The wire spacing is 1.8 mm and the anode-cathode gap is 1.4 mm. The calculated capacitance between wire and strip plane via carbon-coated cathode plane is 11 pF per metre, and the capacitance between two wires is 6.5 pF per metre. The total capacitance of an anode signal source is then approximately 11 pF × 10 + 6.5 pF × 2 = 123 pF per metre of wire length (when 10 wires are ganged together). The wire length varies for different chamber types and even within a chamber because of its trapezoidal shape. The length varies from 50 cm to 170 cm, while the size of the wire-group varies from 5 to 32 wires. The detector capacitance, that contributes to preamplifier noise, is the capacitance of an anode signal source and a HV blocking capacitor (C_{HV}) in series. Therefore the detector capacitance is less than C_{HV} (235 pF). We take it to be between 30 pF and 170 pF.

The TGC cathode is a thin layer of high-resistive carbon paint. There is a 1.6 mm thick dielectric layer of FR4 between the cathode and the readout strips. The width of the readout strip varies since it is fan-shaped. Different chamber types also have different read-out strip widths. The minimum strip width is 15 mm and becomes as wide as 53 mm. The length of a strip is also not constant, varying between 1.2 m and 2.3 m. Longer strips are, however, narrower. Figure 2-3 shows the strip signal path with capacitive coupling between adjacent strips both directly (C_{SS}) and via the carbon resistive plane. It is modeled by two capacitances (C_{SC}) connected together by the carbon resistance plane with resistance value of R_{SS}. Since C_{SC} is the order of nano-Farads, this R_{SS} forms a source of parallel noise. Owing to the long length of the strips and the narrow gaps between them, R_{SS} can be not very large. With a surface resistivity of 1 MΩ per square, R_{SS} is around 2 kΩ. When R_{SS} is above 1 kΩ, the noise contribution from R_{SS} is significantly smaller than that from the amplifier.

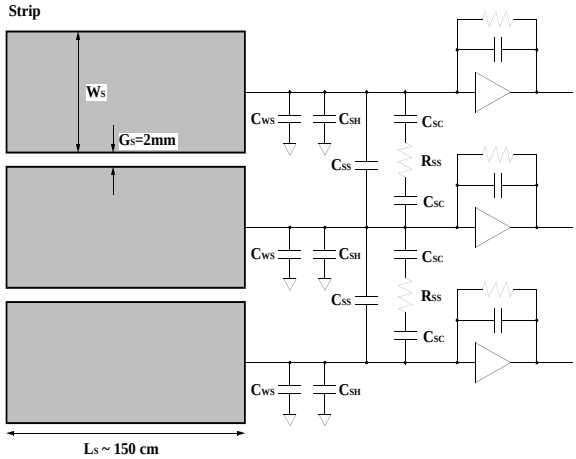

Figure 2-3 Electrical model of strips, showing coupling between neighbouring strips.

Detector capacitance of a strip is a sum of capacitance between strip and wires (C_{WS}), capacitance between strip and strip via honeycomb (C_{SH}), and capacitance of strip to adjacent strips (C_{SS}). Major contribution to the capacitance is C_{WS} that is proportional to the strip area. We estimate the capacitance of the strip signal source to be between 170 pF and 260 pF.

Both of the capacitances of the wire and the strip are significantly higher than those of ordinary drift chambers. The propagation velocity of the wire signal is around 27 cm / ns and the strip is around 15 cm / ns. Table 2-2 summarizes the detector and signal parameters of the TGCs.

Table 2-2 Detector and signal parameters of TGCs

Anode wire length	0.5 ~ 1.7 m	Detector capacitance (wire)	30 ~ 170 pF
Number of wires per group	5 ~ 32	Detector capacitance (strip)	170 ~ 260 pF
Strip width	15 ~ 53 mm	Wire propagation velocity	27 cm / ns
Strip length	1.2 ~ 2.3 m	Strip propagation velocity	15 cm / ns
Wire-group capacitance	35 ~ 620 pF	Total wire signal (electrons in 5 clusters)	1×10^7
HV blocking capacitor for wire	235 pF	Total strip signal (electrons in 5 clusters)	$2.5 \sim 5 \times 10^6$

3 Timing considerations

It is the arrival timing of electrons in the first cluster that determines the signal timing. With two electrons in one cluster, a gas gain of 10^6 and assuming that one-quarter of the avalanche charge is observed with fast shaping, the charge determining the timing, Q_S is:

$$Q_S = 2 \times 10^6 \times \frac{1}{4} = 5 \times 10^5 \text{ electr}$$

For such a Q_S value, the time jitter σ_t and signal-to-noise ratio S/N are:

$$\sigma_t = \frac{ENC}{Q_S} \times t_r \qquad \text{and} \qquad \frac{S}{N} = \frac{Q_S}{ENC}.$$

Assuming the signal rise time t_r after pulse shaping to be 10ns and the Equivalent Noise Charge, ENC, to be 1×10^4 electrons (see Section 4 below),

$$\sigma_t = 0.2 \text{ ns} \qquad \text{and} \qquad S/N = 50 .$$

Hence the contribution from the ENC value is not a serious one for the timing when Q_S is constant. If we set the threshold level to be 5 times larger than the ENC (which will be 1/10 of Q_S), Q_{th} will be 5×10^4 electrons.

The time walk t_W due to a fluctuation of Q_S is

$$t_W = \frac{Q_{th}}{Q_S} \times t_r = \frac{5 \cdot 10^4}{5 \cdot 10^5} \times t_r = 1 \text{ ns}$$

where the minimum Q_S of 5×10^5 electrons was used. The larger the Q_S value, the smaller the value of t_W.

However, this is for anode signals. From the geometrical consideration, the strip signal is smaller than its corresponding anode signal by a factor of 2 (at the center of a strip) to 4 (at the strip boundary). So the time walk for the strip signal is also 2 to 4ns. Since the intrinsic time jitter of the TGC itself is larger than 20nsec for normal-incident tracks, a few nanoseconds time jitter from the front-end electronics does not contribute to the overall performance of the system. This has indeed been verified with the full-sized prototype chambers, where time resolution of the strip is similar to that of the wire. See Figures 4-18.

4 Amplifier and discriminator

4.1 Technology choice

Four channels of amplifiers and discriminators are integrated in one chip. Since about 400,000 channels are produced, reliability and cost are of the prime concern. Taking into account the relatively large detector capacitance and the requirements of the fast shaping and low noise on the amplifier, transistors with large transconductance, g_m, are preferred [5,6]. We chose the amplifiers based on bipolar transistors. The chip has been developed in collaboration with SONY Corporation, using its bipolar 'Analog Master Slice Process'. This semi-custom process provides prefabricated NPN and PNP transistors, resistors, and capacitors. A designer must use these elements when designing circuits. The chip we used contains 850 NPN transistors, 384 PNP transistors, 1738 resistors and 42 capacitors, totaling approximately 1,000 effectively usable elements in each chip area. Characteristics of the transistors are given in Table 4-1. Availability of the low-noise NPN transistors with base-spread resistance $r_{bb'}$ = 17.5Ω was one of the motivations to use the process. Capacitors are of 2 pF and 20 pF values totaling 408 pF (Metal Insulator Semiconductor, MIS capacitor). Resistors are either 8 kΩ or 2.5 kΩ (poly-silicon), 297 Ω (diffused) and 129 Ω (diffused).

Table 4-1 Transistors in the Master Slice Process

Transistor	h_{FE}	f_T (MHz)	$r_{bb'}$ (Ω)	C_{BE} (pF)	C_{BC} (pF)	C_{CS} (pF)
Double Base NPN	120	3200	400	0.093	0.082	0.357
Low-noise NPN	120	950	17.5	9.11	2.90	8.15
Power NPN	125	3000	77.3	1.53	0.996	4.77
Double Base PNP	110	300	300	0.045	0.126	0.954
Power PNP	100	350	57.9	1.25	0.901	4.77

4.2 ASD IC development

4.2.1 Design

We plan to use the same ASD for both wire and strip signals. A block diagram of the ASD chip is shown in Figure 4-1, with schematics in Figures 4-2 and 4-3. Its first stage is a common-emitter cascade charge-amplifier. The input stage of the preamplifier is implemented with the low-noise NPN transistors with $r_{bb'}$ of 17.5Ω. The relatively large capacitance of the transistor (higher than 10 pF) disfavors the use of the transistors in common-base configuration which is usually employed in preamplifiers for chambers. The integration constant is set to be 16 ns. The gain of the preamplifier stage is approximately 0.8 V / pC. An emitter follower output of this preamplifier stage is provided for monitoring.

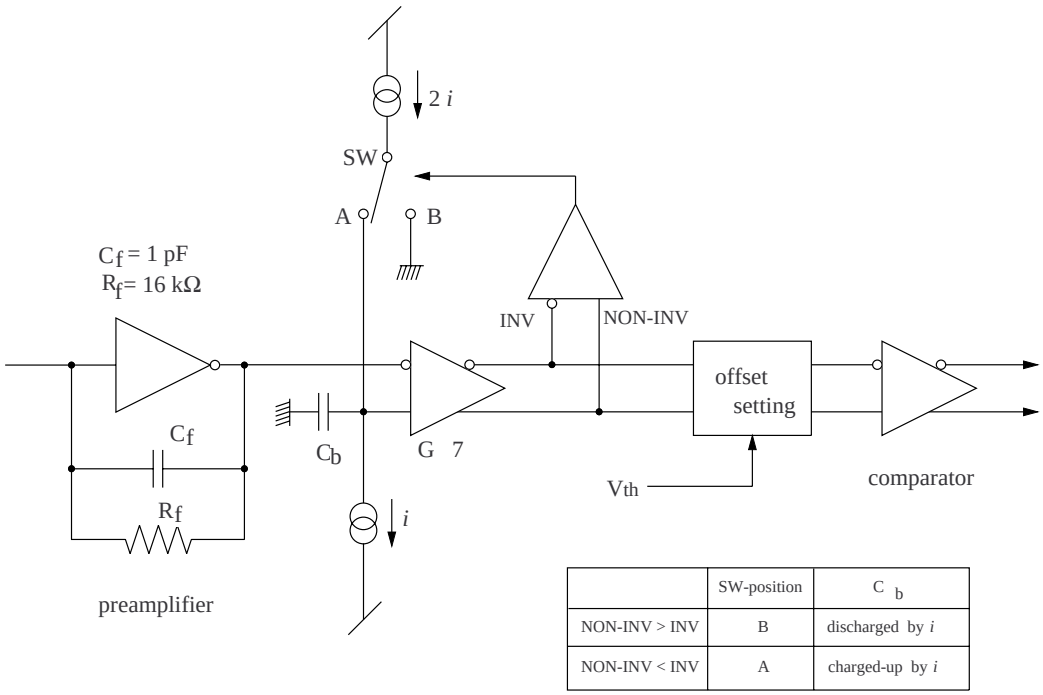

Figure 4-1 Block diagram of the ASD chip.

The second stage consists of a main-amplifier with a baseline restorer and differential outputs. The main-amplifier section has a gain of 7. Depending on the output differential signal level seen by the switch control section, the switch is connected to the “A” side or the “B” side (see Figure 4-1). When the switch is connected to the A side, the capacitor C_b will be charged from the current source by the amount of “*i*”. When the switch is connected to the B side, the capacitor will be discharged by the amount “*i*”, resulting in stabilized DC output levels, or a baseline restoration. In other words, the circuit makes the baseline level of the differential outputs from the main-amplifier to be equal.

Following the main-amplifier is an offset setting circuit which transforms the main-amplifier outputs to the levels required at the inputs to the comparator, where offset voltage is controlled by DC voltage (V_{th}) supplied from outside of the chip. The comparator is shown in Figure 4-3. Its outputs conform to the Low Voltage Differential Signalling standard, LVDS [7], to assure driveability and immunity against noise and minimizing power. By design, this circuit can be used for both wire and strip signals by setting an appropriate threshold level. Table 4-2 is a summary of this chip’s characteristics.

4.2.2 Simulation

Figure 4-4 shows the result of a PSPICE simulation of the preamplifier output, the main-amplifier differential outputs, and the comparator LVDS outputs against impulse inputs of ±0.1 to ±0.5pC charge. Dynamic range (non-saturated range) of the preamplifier against negative / positive impulse charge inputs is from –1.2 to +2.0 pC. The slewing rate of the preamplifier also limits the linearity for large positive charge inputs. The dynamic range and the gain of the preamplifier observed at the buffered output (open emitter) depends on the external load and is less than that of the internal one. The circuit can successfully accept signals of 5 MHz or higher frequency.

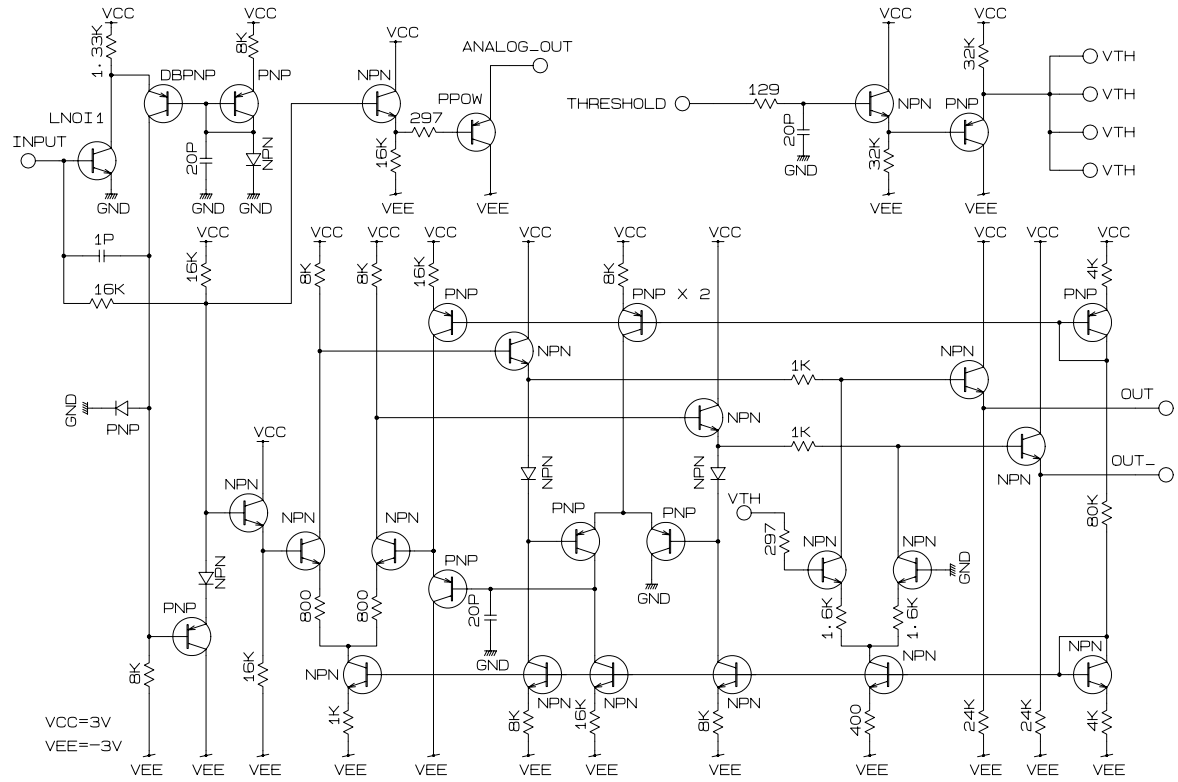

Figure 4-2 Schematic diagram of the preamplifier, main-amplifier and baseline restorer.

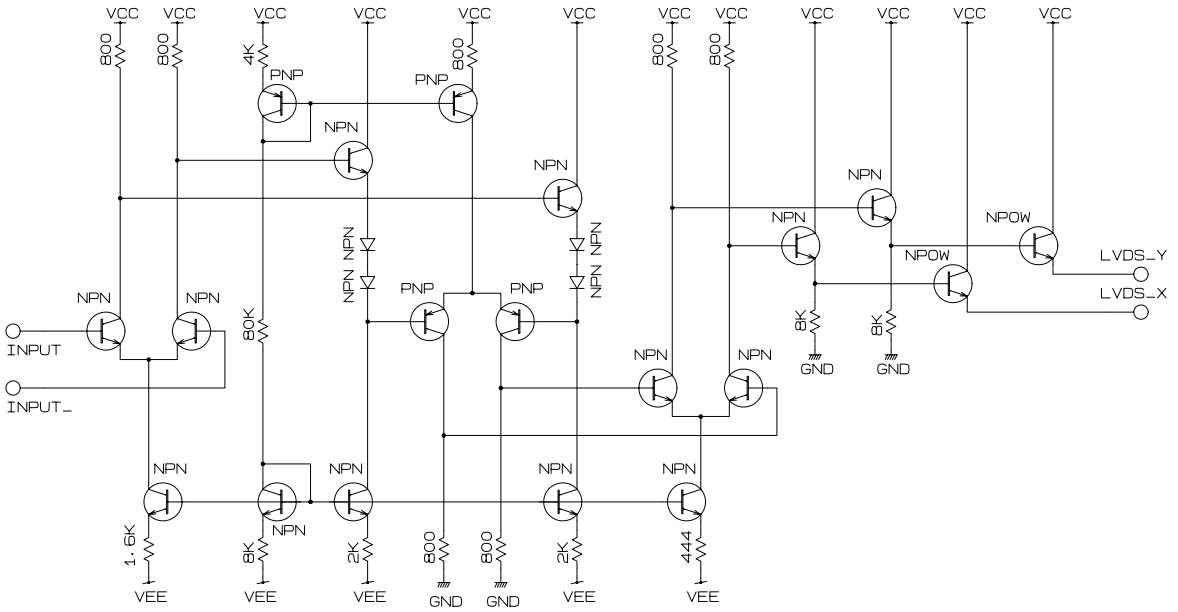

Figure 4-3 Comparator schematic diagram.

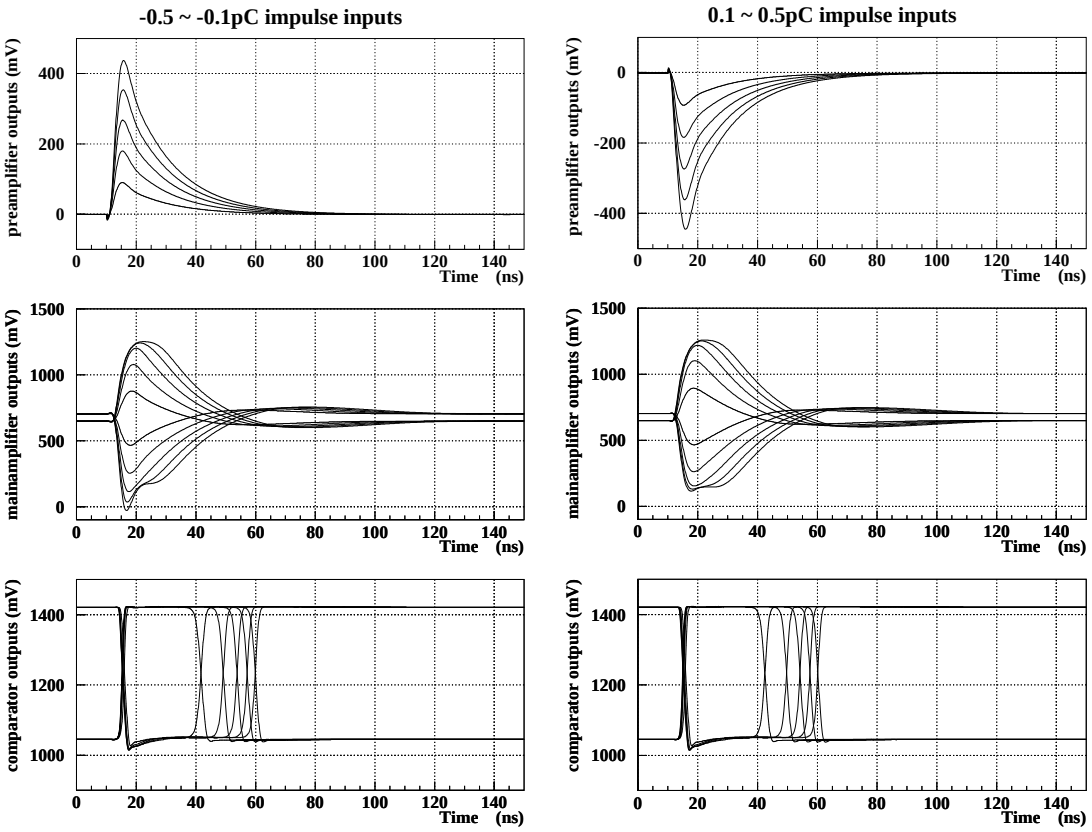

Figure 4-4 SPICE simulation of (1) the preamplifier output, (2) the two main-amplifier differential output signals, and (3) the two comparator differential output signals (LVDS).

Figure 4-5 shows the calculated equivalent-noise-charge (ENC) as a function of detector capacitance. At 150 pF input capacitance, ENC is 7500 electrons r.m.s.

Figure 4-6 shows the input impedance of the preamplifier as a function of input frequency. The input impedance is around 80Ω for input signals of up to 100 MHz.

Figure 4-7 shows offset voltage at the differential inputs of the comparator as a function of supplied voltage (V_{th}). This offset value corresponds to the real threshold voltage for the comparator. The figure shows that the real threshold voltage can be varied from –0.25V to +0.25V and the real threshold voltage is approximately one half of the applied voltage to the V_{th} pin. Positive voltage should be applied for the cathode signal and negative voltage for the anode signal. For example, when one sets the threshold at 50,000 electrons for anode signals, V_{th} is -90 mV.

We also made simulation taking into account the fluctuation of the parameters in the process among various production lots. The h_{FE} of the transistor fluctuates from 55 % to 170 % and the V_{BE} by ± 30 mV. The fluctuation of the poly-silicon resistor is ± 20 %, and capacitance of the MIS capacitor is ± 8 %. The results from the simulation don't indicate any instability of the preamplifier and the main-amplifier. The gain deviation of the preamplifier is from -7 % to +5 %. When 50 % degradation of h_{FE} from the radiation damage is assumed, additional 10 % decrease of the gain is expected.

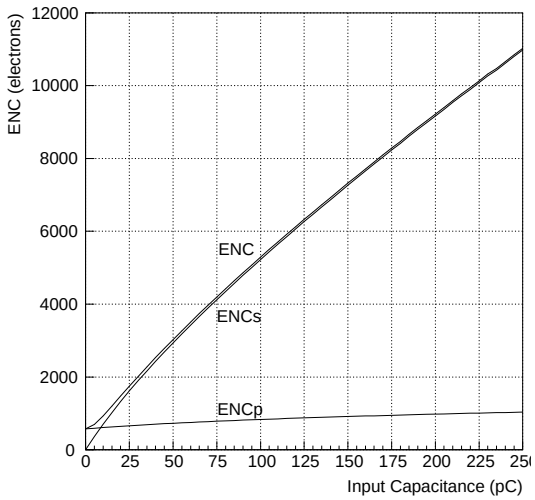

Figure 4-5 Calculated equivalent noise charge, ENC, as a function of detector capacitance. ENC = $\sqrt{(ENC_s^2 + ENC_p^2)}$.

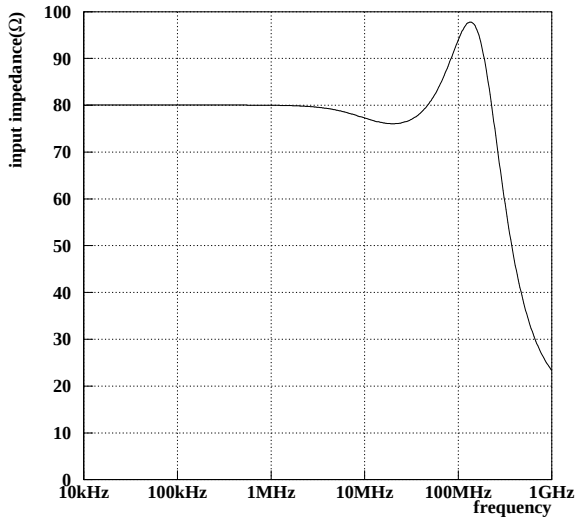

Figure 4-6 Input impedance of the preamplifier as a function of input frequency.

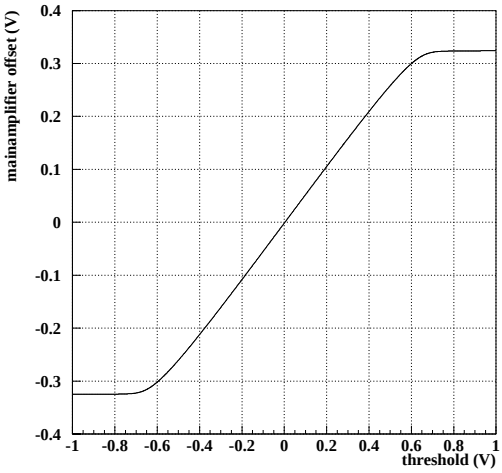

Figure 4-7 Offset voltage at the differential input of the comparator as a function of supplied voltage (V_{th}).

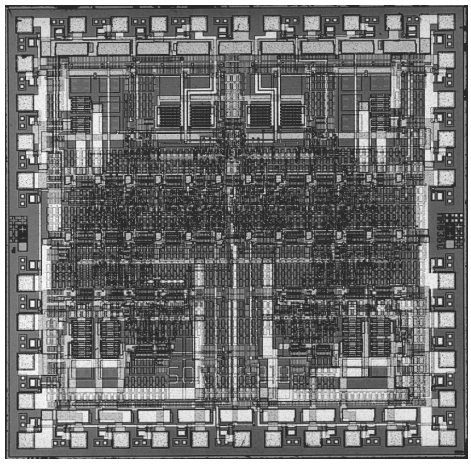

Figure 4-8 Photograph of the 4-channel ASD chip. The die size is 3.1 mm x 3.1 mm.

4.2.3 IC layout

Four channels of ASD circuits are fabricated on a 3.1mm×3.1mm die as shown in Figure 4-8. The pin assignment of the ASD IC using a QFP48 package is shown in Figure 4-9. Detailed dimensions of the package are shown in Figure 4-10. The threshold voltage is common to all four channels. In the layout work of the IC, much attention was paid to reduce interference between analog and digital signals and cross-talk among channels. Both ground and power patterns and pins for the analog part are separated from those for the digital part. In Figure 4-9, power for channels 1 and 2 is supplied from the pins on the left side (pins 39, 41, 44, 46) and power for channels 3 and 4 is supplied from the pins on the right side (pins 15, 17, 20, 22). The pin assignment of the package is right–left symmetric, so that designing the PC board layout is easier. For

protection against static charge, diodes are inserted between all the I/O pads and the highest positive/negative voltage except for the ground and DC power pads.

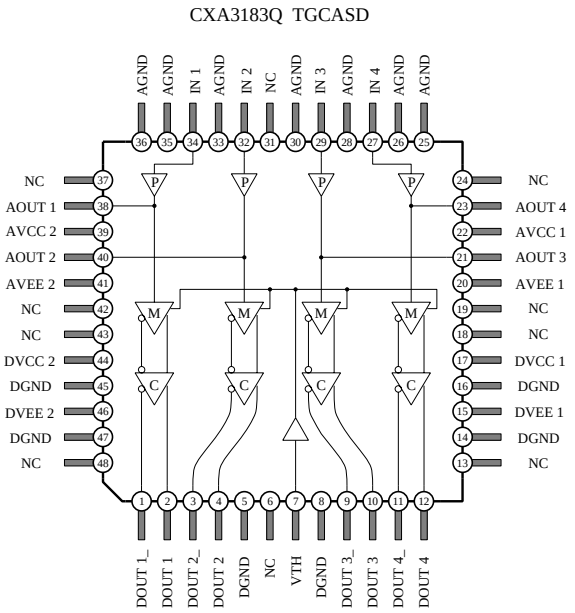

Figure 4-9 Pin assignment of the ASD IC.

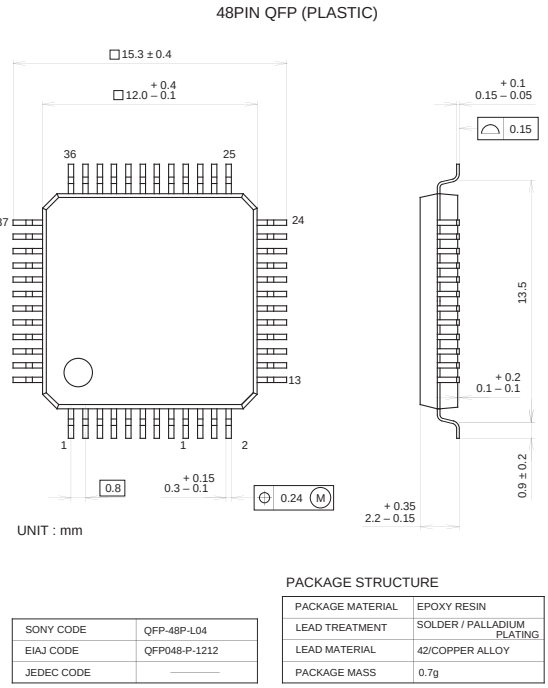

Figure 4-10 Detailed dimensions of the package.

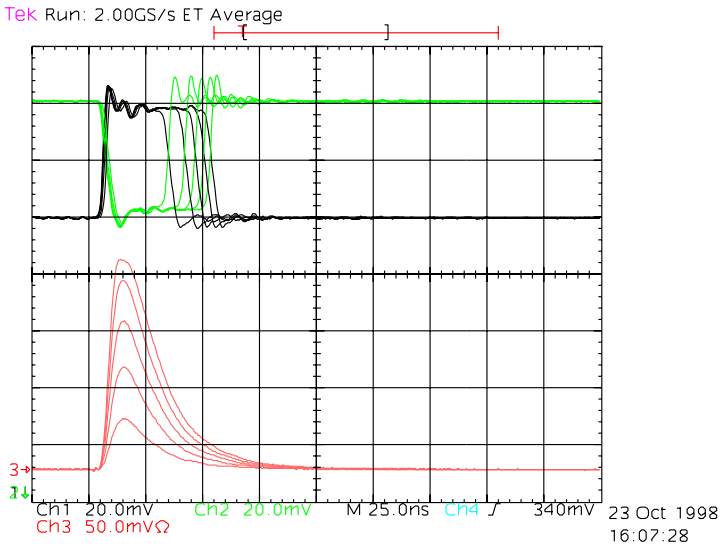

Figure 4-11 Oscilloscope trace of the preamplifier external output for inputs from 0.1 to 0.5 pC.

4.2.4 Performance

The analog and digital signals from the ASD chip for inputs from –0.1 pC to –0.5 pC are shown in Figure 4-11. The overall time walk of the comparator outputs due to the input charge variation of between 0.1 pC to 2 pC is less than 2 ns, when the threshold is set at 0.01 pC equivalent, as shown in Figure 4-12. We also tested the performance of the main-amplifier and the comparator using prototype chips where the preamplifier, the main-amplifier and the comparator were fabricated separately for independent study. In order to check comparator characteristics, we measured propagation delay while changing conditions such as: varying over-the-threshold-voltage of the input pulse for fixed rise time; varying over-the-threshold-voltage of the input pulse for fixed slope; varying rise time for fixed input pulse height. The results show that the time walk of the comparator was less than 2 ns under these conditions. These results agree with the PSPICE simulations.

The temperature dependence of the preamplifier gain was approximately $-0.08\%/°C$. The feedback (integration) capacitor of the preamplifier is supposed to be the major contributor to the temperature dependence.

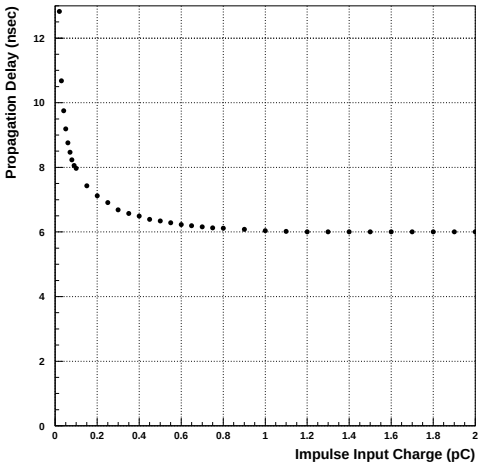

Figure 4-12 Overall time walk of the comparator outputs.

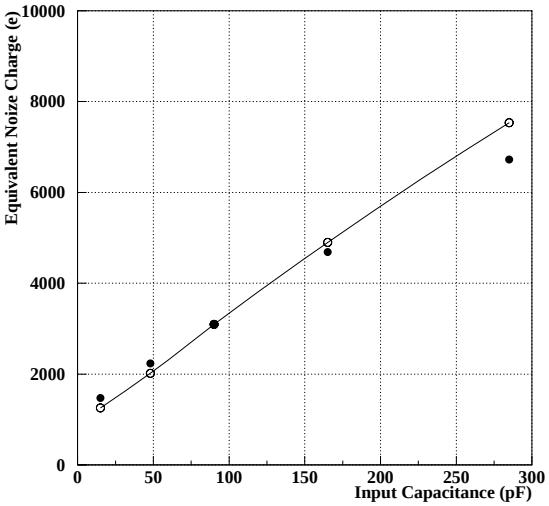

Figure 4-13 ENC as a function of input capacitance. Closed-circles are the measured values and open-circles are the calculated values.

The equivalent noise charge (ENC) was measured as a function of input capacitance as shown in Figure 4-13. We calculated the ENC using design the parameters of the preamplifier and the measured impulse response of the evaluation system. The calculation reproduces the measured data with the base-spread resistance $r_{bb'}$ of 15Ω and the h_{fe} of 90.

Cross-talk among channels was less than 0.5% when the preamplifier analog output pins were left open. If the open-emitter buffer for the analog output drives a 50Ω load, the cross-talk becomes 3 times larger[1]. The influence of the digital part on the analog part was much less than the cross-talk between channels.

1. The analog output is expected to be used only for monitoring one channel per chamber.

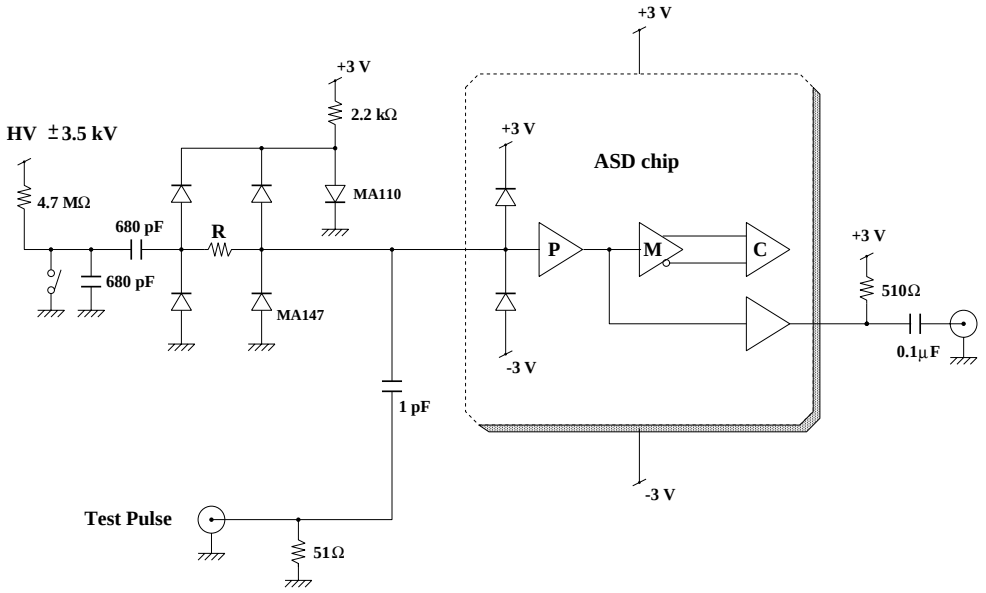

Figure 4-14 Test set-up for external protection circuit.

Immunity against discharge of static charge was examined by SONY according to its standard test procedure prior to production and was proved to be safe. However the on-chip I/O pad protection alone may not be enough to protect the ASD from high voltage discharges in the chambers. We tested external protection circuits as shown in Figure 4-14. The capacitor was charged up to plus or minus 3.5 kV. Discharge was made by the switch to simulate the chamber spark and we checked the effect to the ASDs. During this test, test pulses were fed to the ASD repeatedly. The capacitors of 680 pF simulate a high voltage blocking capacitor and detector capacitance. The resistor "R" between the diodes is very effective in protecting the ASD. However we want to set the value of the resistor as low as possible, since the resistor can be a series noise source. Without the resistor, the ASDs were destroyed after a few discharge cycles of the positive high voltage. With a 10 Ω resistor, the ASD could survive more than 50 discharges. We have established an appropriate protection circuit for immunity against the discharges

Table 4-2 CXA3183Q TGC ASD chip characteristics

SONY Analog Master Slice (bipolar semi-custom)
Preamplifier gain of 0.8 V / pC
16 nsec integration time
Input impedance of around 80 Ω
Open-emitter analog outputs
Main-amplifier with a gain of 7
Baseline restoration circuits
Comparator with LVDS outputs
ENC ≈ 7500 electrons at C_D = 150 pF
4 channels in a QFP48 plastic package
Threshold voltage: common for all 4 channels
Required voltage: ±3V, GND
59 mW / ch when driving a 100 Ω load (+3V:16.4 mA, -3V: 3.25 mA, 46 mW in ASD chip and 13 mW at LVDS receiver end)

Table 4-2 is the summary of the characteristics of the ASD chip. Pre-production samples (1,200 chips, without inspection by SONY before shipment from its production line) satisfied the specification except for 23 chips, which were found dead and were rejected prior to fabrication. These samples were used for TGC beam tests at KEK and at CERN.

4.3 ASD Board development

The 16-ch ASD Board was designed and built for both wire signals and strip signals from the TGC. Each board contains 4 ASD ICs with protection circuits shown in Figure 4-14 and a test pulse circuit that receives a test pulse (a differential squire-wave analog signal) and distributes a charge impulse to each channel. The amount of the input charge is proportional to the amplitude of the input test pulse. The board design is common for all TGC chambers. It is coupled to a narrow adapter board which is attached to the chamber. The adapter board converts the wire-group (or strip) pitch on the chamber side to the pitch of the input connector on the ASD Board. A 32-pin right-angle SIP connector (male) is used for the inputs of the ASD Board. Each pin is alternately assigned to a signal and ground. A couple of copper plates on both sides of the ASD Board mechanically attach the board to the adapter board with screws and connect ground of both boards securely. LVDS logic signals from the ASD Board are transmitted through a 20-pair twisted-pair cable and a preamplifier output through a LEMO type connector. DC power, ground, threshold voltage (common over a channel) and test pulse are supplied back to the ASD Board via the same twisted-pair cable. Pin assignment of the flat cable connector is in Appendix.

In order to reduce the production cost, the board was designed as a 2-layer PCB. Devices are surface mounted except for connectors on only one side. The photograph of the ASD Board is shown in Figure 4-15. The detailed schematics, PC board layout and parts list for the ASD Board are in Appendix.

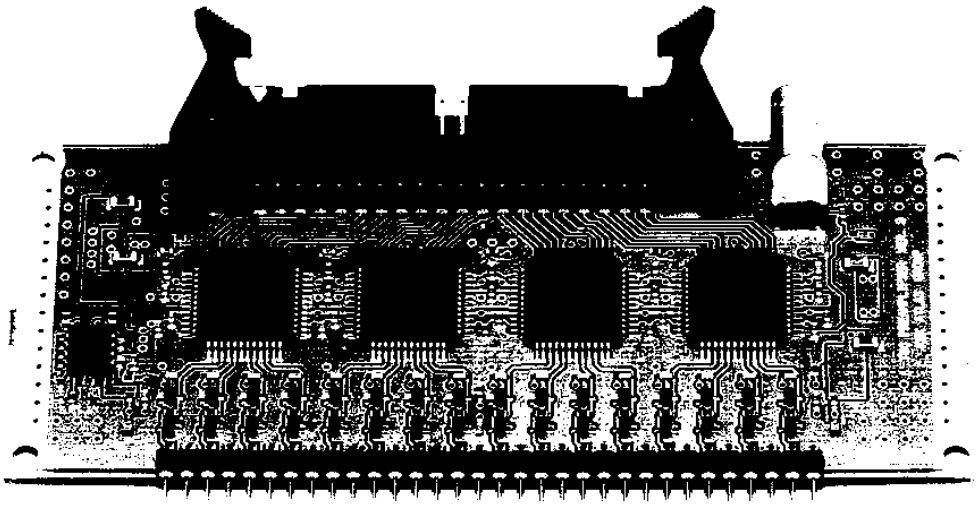

Figure 4-15 Photograph of the 16-CH ASD Board.

4.4 Beam tests

We tested TGCs with the prototype ASD ICs at KEK in April 1998 and at CERN in September 1998. At KEK, we used pion beams with essentially no background hits. Whereas at CERN the chamber was tested under gamma irradiation.

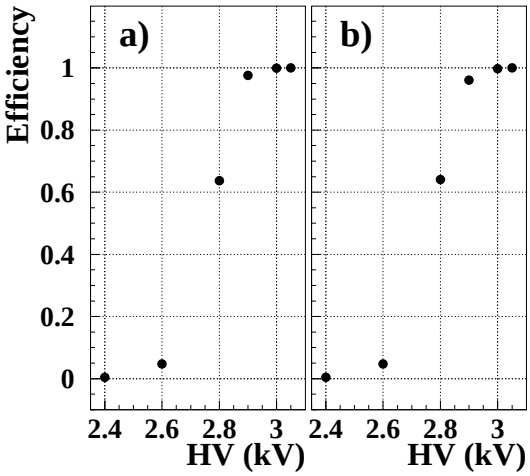

Figure 4-16 Detection efficiency as a function of applied high voltage for the wire signal (a), and the strip signal (b).

4.4.1 Test at KEK

We tested one doublet (two TGC layers) and one triplet (three TGC layers). There were 32 wire groups in each TGC layers. Except for the middle layer of the triplet, there were 32 strips in each TGC layer. In case of the middle layer of the triplet, only the wire signals were readout. Typical dimensions of the wire group were 38 mm (21 wires) in width and 1.5m in length; the strip dimensions were 46 mm in width and 1.2m in length.

Each ASD board was housed in a Faraday cage and was electrically shielded. A flat ribbon cable with 40 lines was used for 16 signal outputs, electric power lines, their returns, test pulse and threshold voltage. The cable was also shielded. We used 11 ASD boards (44 ASD ICs) in total. The threshold voltage was set to be five times of the ENC (rms) of the ASD.

Beam went through the chambers at normal incidence unless otherwise stated. Figure 4-16 shows the detection efficiency versus applied high voltage on the wires. The efficiency plateau starts at around 2.9kV for both wire and strip signals. The results shown here are those at 3.0kV of applied voltage unless otherwise stated.

The noise counting rate normalized in the unit area was about $0.1\,Hz/cm^2$ for the wire and $0.3\,Hz/cm^2$ for the strip signal. These are to be compared with uncorrelated hits at the TGC trigger stations, which is typically $5\,Hz/cm^2$ at the nominal LHC luminosity [8].

The timing distributions of the wire signal for various incident angles are shown in Figure 4-17. The incident angle is defined as an angle between the beam direction and the normal of the wire plane rotated around an axis parallel to the wire. The "95% time jitter" is defined as a time window into which 95% of events enter. The time jitter depends on the

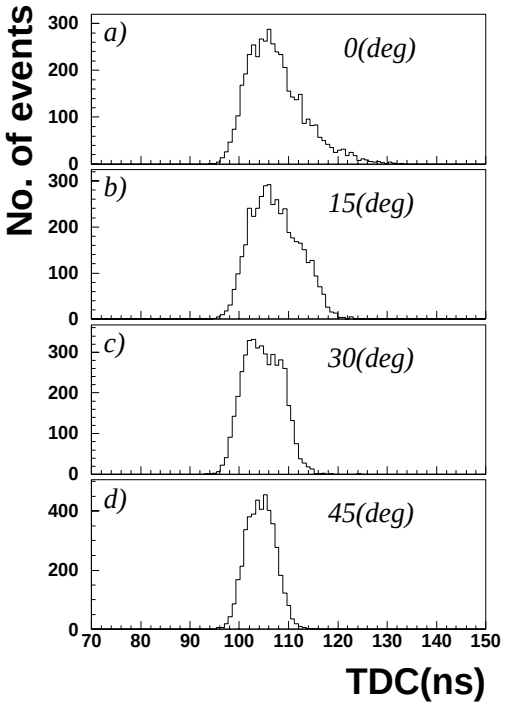

Figure 4-17 Timing distribution of the wire signal for various incident angles.

applied high voltage on the wire as shown in Figure 4-18, where particles enter the chamber normally. In the case of normal incidence (0°), some particles pass the weak electric field region between the two wires. Those particles make the tail of the time distribution. If the chamber is inclined, at least some of the ionized electrons are produced in the higher electric field. Therefore, the more the chamber is inclined, the more the tail is reduced. This trend is clearly seen in Figure 4-17. The 95% time jitter dependence on the incident angle is shown in Figure 4-19. For the muon triggering in the endcap region, the TGCs cover a pseudorapidity region of $1.05 < |\eta| < 2.4$. So the relevant incident angle is larger than 10° in practice.

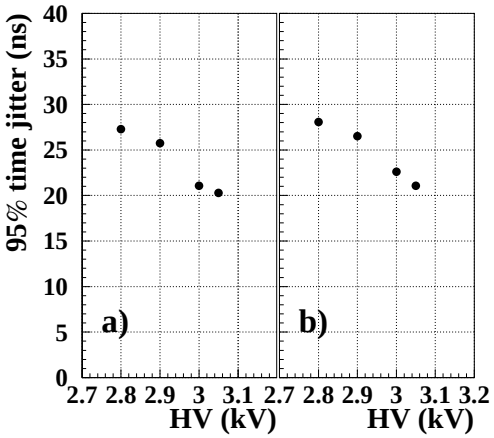

Figure 4-18 The 95% time jitter for normal-incident tracks as a function of applied high voltage for the wire signal(a), and the strip signal(b).

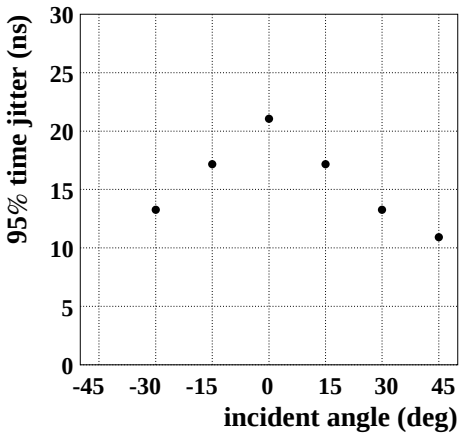

Figure 4-19 Incident angle dependence of the 95% time jitter for the wire signal at 3.0kV.

These results are consistent with the ones using hybrid ASD circuits tested before. During the beam test for about 10 days, the front-end system worked stably and showed no problem. As a summary, the performance of the ASD chips were proved to be satisfactory.

4.4.2 Test at CERN

We also tested a doublet TGC under high background environment at CERN in September 1998. We used the muon / photon test facility at X5 in the West Experiment Area of the SPS. The threshold voltage was set at 5 times of the ENC of the ASD. The chamber was irradiated almost uniformly over the entire region with the maximum hit rate of $770\,\mathrm{Hz/cm^2}$. The typical estimated hit rate at the nominal LHC luminosity is $30\,\mathrm{Hz/cm^2}$ at the trigger stations, and less than $150\,\mathrm{Hz/cm^2}$ at the inner station at $z = 7\,\mathrm{m}$. Preliminary results are shown in Figure 4-20 and Figure 4-21. The chamber was inclined by 20° with respect to the beam direction. Figure 4-20 shows the efficiency versus applied voltage for the wire signal under various background conditions. The rate dependence of the efficiency at applied voltage of 3.0kV is shown in Figure 4-21. The efficiency is high enough even at five times the predicted background rate at the inner station, and 25 times at the trigger stations. In summary, the ASD chips together with the Module-0 TGC perform as expected in the real ATLAS environment.

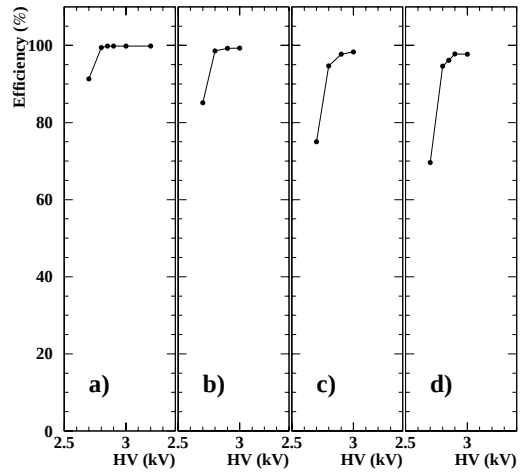

Figure 4-20 Efficiency as a function of applied HV for the wire signal under various background conditions: a) no irradiation, b) 125 Hz/cm^2, c) 500 Hz/cm^2, and d) 770 Hz/cm^2.

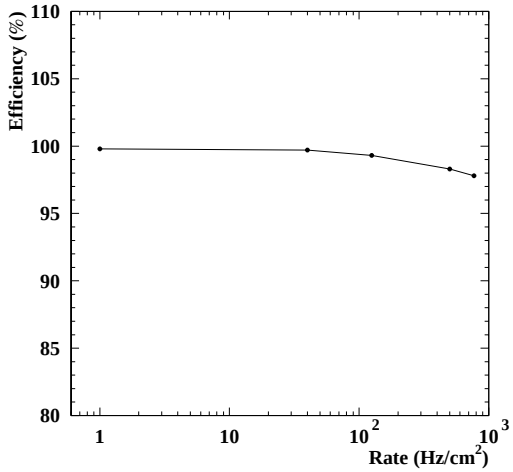

Figure 4-21 Efficiency versus background rate for the wire signal at 3.0kV.

4.5 Aging test

The reliability study was performed using the accelerated aging method. Expected life is affected by operating temperature. Generally, each 10 ˚C reduction in temperature will double the expected life. The formula for calculating expected life at lower operating temperatures is as follows;

$$L_2 = L_1 \times 2^{(T_1 - T_2)/10}$$

where,

L_1 : Tested life at temperature T_1°C

L_2 : Expected life at temperature T_2°C

T_1 : Aging-test temperature (°C)

($T_1 <$ maximum operating temperature of the device)

T_2 : Actual operating temperature (°C)

For the device to survive 10 years at 25 ˚C (expected operation temperature), the device must survive 5.3 months at the aging-test temperature of 70 ˚C.

Four 16-ch ASD Boards with analog outputs were exposed to 70 ˚C for 6 months. During the test, they were continuously powered and test pulses were fad into them and analog and digital signals were observed. All the ASD Boards survived the aging test without any visible sign of degradation neither any signal degradation. It was proven that the life time of the ASD Board at 25 ˚C is expected to be longer than 10 years.

5 Radiation tolerance

5.1 Requirements

Much of the volume of the ATLAS detector will be in an extremely harsh radiation environment. Although even the highest radiation level in areas where the TGC trigger electronics is located (that closest to the interaction point) is far from the most extreme in ATLAS, it still offers challenges that must be met to ensure the long-term performance of the trigger.

Using data from a simulation of the expected radiation environment in ATLAS [9], radiation levels at the TGC wheels are summarized in Table 5-1.

Taking into account the uncertainty in the estimation, a safety factor of four is required [9]. The bipolar transistors, which have a higher sensitivity to radiation damage, require an additional factor of 1.5 for the neutron flux and a factor of five for the ionizing dose.

The radiation tolerance criteria at the worst location of the TGC trigger station for 10 years running are summarized in Table 5-2.

Bipolar technology was used for the ASD chip and sub-micron CMOS technology will be used for the trigger and read-out gate arrays. Such technologies have already been investigated for radiation tolerance [10]. In our application, special radiation tolerant processes were not chosen due to difficulties in both availability and cost. The SONY P23 standard-process ICs were checked for radiation tolerances.

Table 5-1 Typical radiation levels per year in the regions where TGC electronics will be located. The two locations correspond to the most and the least extreme in terms of radiation environment

	Worst Location	**Best Location**
Neutrons, $n/cm^2/yr$	9.7×10^{10}	3.1×10^{10}
1 MeV equivalent neutron $/cm^2/yr$	2.0×10^{10}	3.6×10^{9}
Dose, Gy/yr	6.2×10^{-1}	2.1×10^{-1}

Table 5-2 Radiation tolerance criteria for chamber-mounted electronics for 10 years LHC running

	CMOS	**Bipolar**
Neutrons, n/cm^2	3.9×10^{12}	5.9×10^{12}
1 MeV equivalent neutron $/cm^2$	8.1×10^{11}	1.2×10^{12}
Dose, Gy	2.5×10^{1}	1.3×10^{2}

5.2 Radiation tolerance test

The front-end electronics boards with the ASD chips will be mounted directly on the TGCs. Therefore the ASD chips will be exposed to a high level of both ionizing (gamma) and neutron radiations. The expected dose and the neutron fluence at the worst location of TGCs in the forward muon trigger station, integrated over 10 years of LHC running with a luminosity of 10^{34} $cm^{-2}s^{-1}$, are 125 Gy and 1.2×10^{12} 1MeV equivalent neutrons$/cm^2$[9]. Note that these values incorporate a safety factor of 4 reflecting the uncertainty of the radiation level estimation, as well as additional safety factors which is specific to the bipolar electronics: 5 on the ionizing rate and 1.5 on the neutron rate[9].

We exposed the ASD chips of the final version to gamma and neutron radiations up to the doses much higher than the above values, and measured the change of gain and noise of the circuits. We also exposed bipolar transistors used in the ASD chips. The manufacturer of the ASD chips supplied us some sample packages containing 5 NPN transistors or 4 PNP transistors each. We measured the direct current amplification factors, h_{FE}, of the transistors for both the biased and unbiased cases.

Futhermore, we tested a couple of component devices of the ASD board, the diodes and video amplifiers. The diodes are used in the protection circuit of the boards and we checked V-I curves to confirm that no reverse breakdown occurred after irradiation. We also measured the gains and ise / fall times of the video amplifers to be used to distribute a test pulse in the ASD Board.

5.2.1 Gamma irradiation (I)

5.2.1.1 Setup

The gamma irradiations were performed at Radioisotope Research Center of Tokyo Metropolitan University. The gamma-ray source was ^{60}Co capable of irradiating a cylindrical volume of 76mm in diameter and 200 mm in height at a rate of 6.7 kGy / hour. Dose was calculated from the irradiation time.

Two packages of NPN transistors and two of PNP were exposed to the radiation. In each package, half of the transistors were biased with I_C kept at 0.5mA during the irradiation, while the other half were unbiased (all the pins were connected to the ground). We measured the h_{FE} of the transistors after a certain irradiation, and then resumed the irradiation to accumulate the dose in the same transistors. This procedure was repeated up to the highest dose.

As for the ASD chips, no bias voltage was applied (all the pins were floated) during the irradiation. Since the measurement on the chips could not be done at the irradiation site, we performed several runs with different irradiation times on different sets of ASD chips, where two chips were irradiated in each run.

5.2.1.2 Result

Irradiation level on the individual transistors were up to the total dose of 20kGy. Figure 5-1 to Figure 5-4 show the results of the h_{FE} measurements as a function of I_C for each of NPN / PNP transistors with / without biasing (one transistor sample for each plot). Taken into account the piece-to-piece difference of h_{FE} for these types of transistors is an order of 10%, there is no significant difference in h_{FE} deterioration between the biased and unbiased cases. Figure 5-5 to Figure 5-8 show the h_{FE} values as a function of dose at I_C = 0.4 mA for all the measured samples. One can see from those plots that degradation in h_{FE} at the dose of 100 Gy is within 10%.

Gain change of the preamplifier part of the ASD chip, as well as the Equivalent Noise Charge (ENC) as a function of the input capacitance, were measured up to the total dose of 30kGy, as shown in Figure 5-9 and Figure 5-10. At a nominal value of the input capacitance (165pF), the ENC values are plotted as a function of dose in Figure 5-11. Changes in both the gain and the ENC after 100 Gy irradiation are within the range of the piece-to-piece variation.

Thus the ASD chips will see negligible effect against the ionizing radiation expected for 10 years of LHC running.

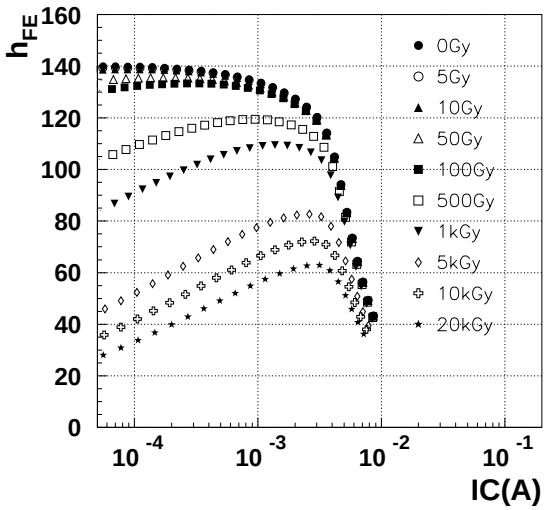

Figure 5-1 Result of gamma irradiation on a NPN transistor. The transistor was not biased during the irradiation.

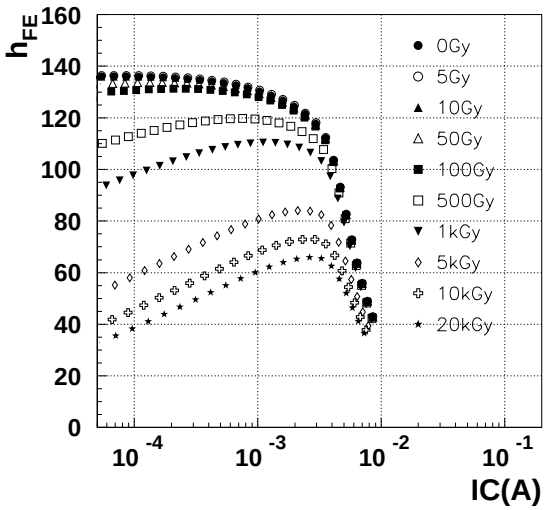

Figure 5-2 Result of gamma irradiation on a NPN transistor. The transistor was biased during the irradiation.

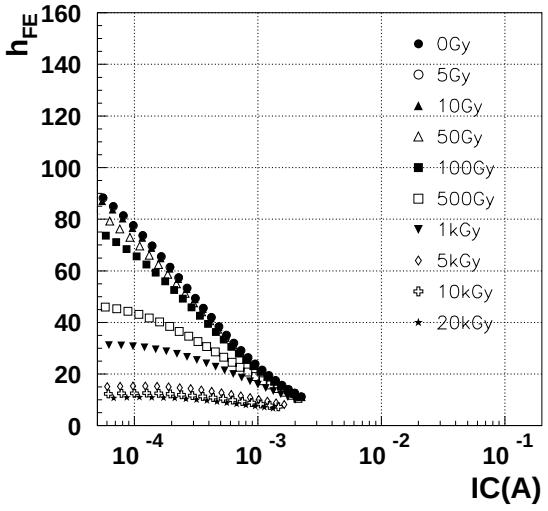

Figure 5-3 Result of gamma irradiation on a PNP transistor. The transistor was not biased during the irradiation.

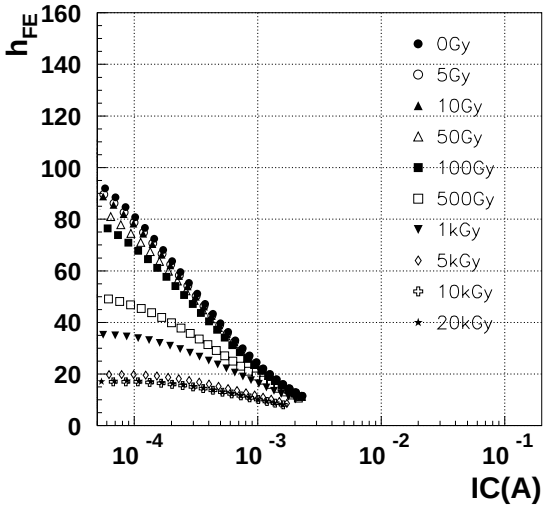

Figure 5-4 Result of gamma irradiation on a PNP transistor. The transistor was biased during the irradiation.

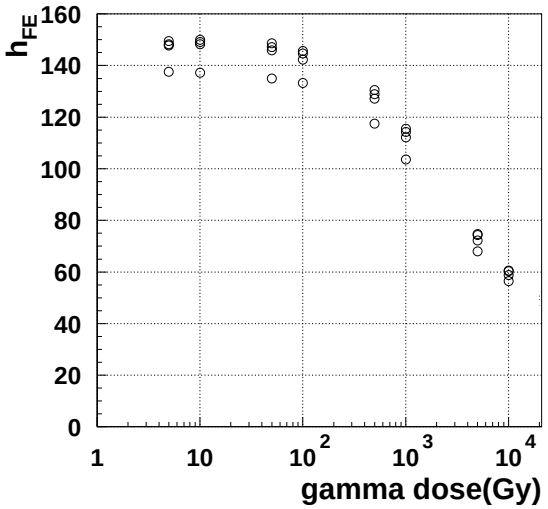

Figure 5-5 h_{FE} values at I_C = 0.4 mA for NPN transistors as a function of dose. The transistors were not biased during the irradiation.

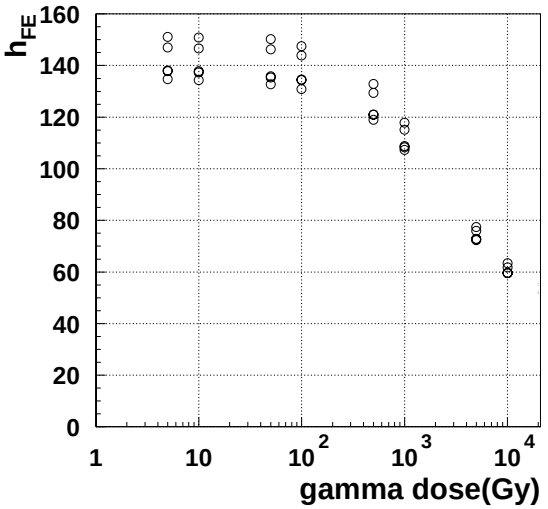

Figure 5-6 h_{FE} values at I_C = 0.4 mA for NPN transistors as a function of dose. The transistors were biased during the irradiation.

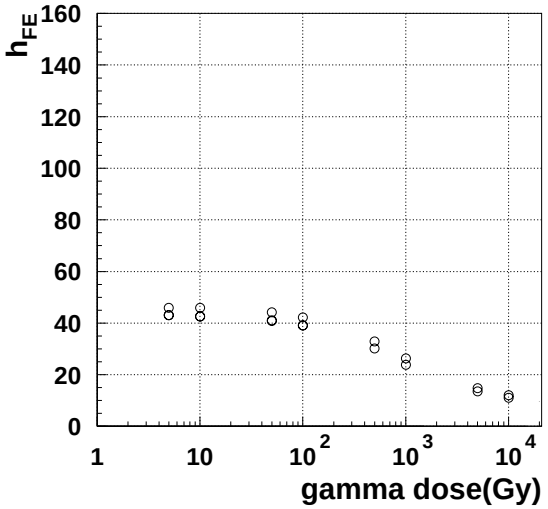

Figure 5-7 h_{FE} values at I_C = 0.4 mA for PNP transistors as a function of dose. The transistors were not biased during the irradiation.

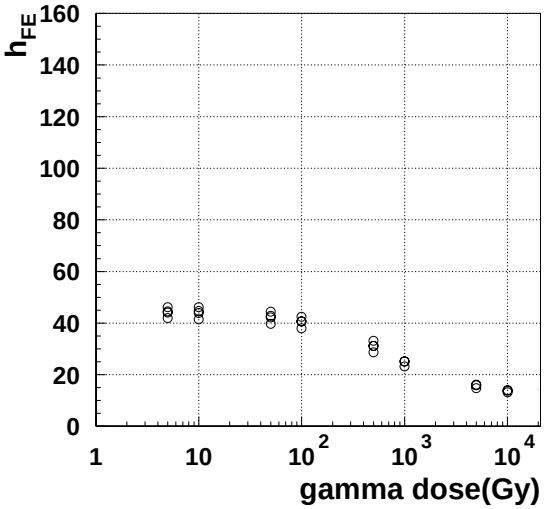

Figure 5-8 h_{FE} values at I_C = 0.4 mA for PNP transistors as a function of dose. The transistors were biased during the irradiation.

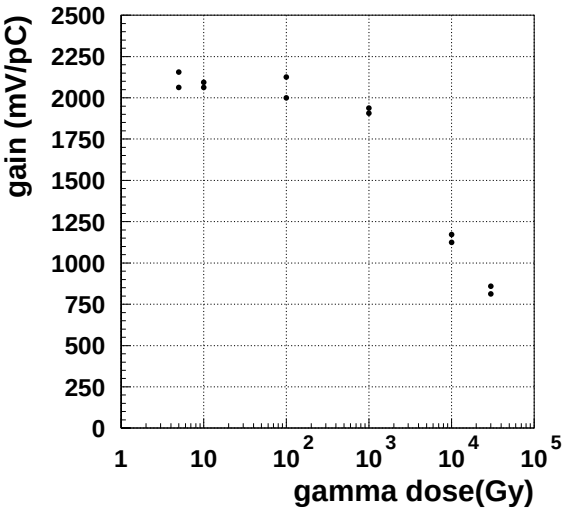

Figure 5-9 Gain changes of ASD chips versus gamma dose.

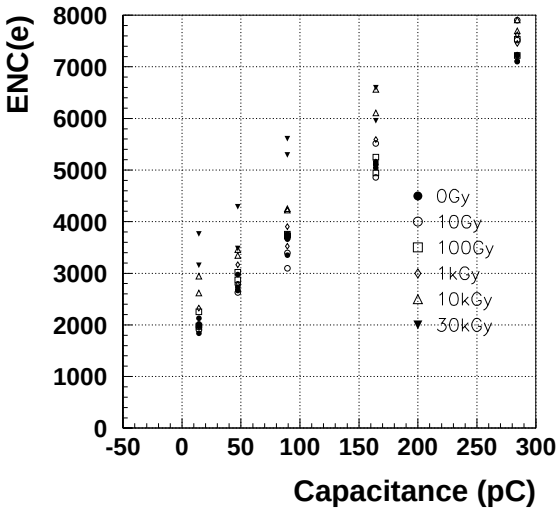

Figure 5-10 ENC values of ASD chips as a function of input capacitance for various doses.

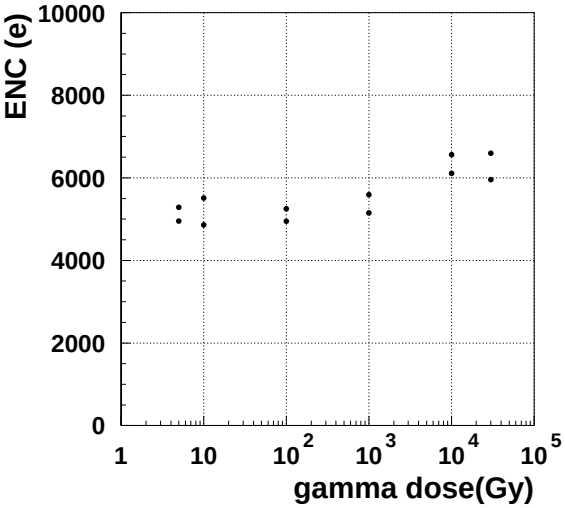

Figure 5-11 ENC values of ASD chips at the input capacitance of 165pF as a function of dose.

5.2.2 Gamma irradiation (II)

In the other gamma-ray irradiation test, we tested the diodes and video amplifiers to be used in the ASD Boards. This test was performed in a similar way to the irradiation test described in section 5.2.1. The main difference between the two tests was the dose rate. Previous irradiation rate was 6.7 kGy/hr, while the same was 5 Gy/hr in this test. Since devices could be damaged by irradiations much more at lower rate, the radiation tolerance at the lower rate (5 Gy/hr) was checked. We have also radiation tested the component transistors in the ASD chips at this irradiation rate.

5.2.2.1 Setup

The gamma-ray irradiation facility at Research Center for Nuclear Science and Technology of the University of Tokyo was used for the test. There was an irradiation table where a cyclinder is placed in the middle. For irradiation, a ^{137}Cs gamma-ray source was mechanically elevated into the cylinder. Tested devices were placed at 90 cm from the source to provide the dose rate of 5 Gy / hr. Total dose was calculated from the irradiation time.

All the tested devices were irradiated until they accumulated a certain dose in each run. Then their properties were checked. The same devices repeatedly received more dose to check for higher dose. Totally seven runs were performed on the same test samples to accumulate up to a total dose of 450 Gy.

In this test, we irradiated four packages each of NPN transistors and PNP transistors. (Each package contains 4 transistors.) For each type of transistors, two of the four packages were connected to a bias circuit and the rest were not connected. Among the packages connected to the bias circuit, half of the transistors were biased keeping I_C at 0.4 mA, while the other half were unbiased (all the pins were grounded). We measured h_{FE} of the transistors during each run.

We tested following diodes: MA111 and MA147 (Panasonic) , 1SS302 (Toshiba) and HSB123 (Hitachi). Eight diodes of each kind were irradiated. All the pins of them were electrically floated during irradiation. After each irradiation run, currents were measured as a function of bias volatage from -10 V to 10 V .

As for the video amplifiers, TL592B (TI), to be used in ASD Boards, eight of them were irradiated and the gain and rise / fall times of the amplifiers were measured after each run.

5.2.2.2 Result

Figures 5-12 to 5-15 show the results of the h_{FE} measurements as a function of I_C for each NPN / PNP transistors with and without biasing. The results were very similar to those shown in the previous gamma-ray test; there is no significant difference in the h_{FE} change between the biased and unbiased samples in this test. We compared the performance of the samples whose pins were grounded with that of the samples whose pins were floated. No significant difference were observed between the two. We also checked the h_{FE} value of biased samples as a function of total dose. When compared with the results in section 5.2.1, no difference was observed in h_{FE} . The degradation in h_{FE} after 100 Gy dose was less than 10%, same as in the previous test.

For the diodes, V-I curves stayed unchanged during the irradiation test. (Typical leak current stayed at 5.5 nA with reverse bias of -10 V.) No significant difference was observed between each product after various values of total dose. No products broke down after any dose level.

Figure 5-16 shows the gain of TL592B as a function of total dose. The first dots in the left of the figure show the gain before irradiation (zero dose). The result shows no significant variation up to the maximum dose. The same was observed on rise time and fall time.

Thus the components of the ASD Board including the ASD chips is expected to survive a total dose equivalent to the 10 years of LHC running. The transistors having been tested at a high dose rate in previous test is now expected to survive at a low dose-rate environment.

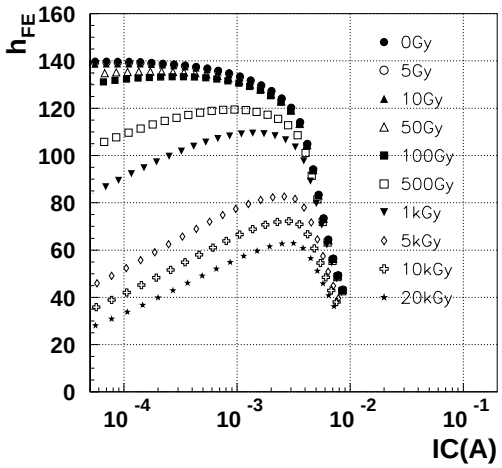

Figure 5-12 Result of gamma irradiation on a NPN transistor. The transistor was not biased during the irradiation.

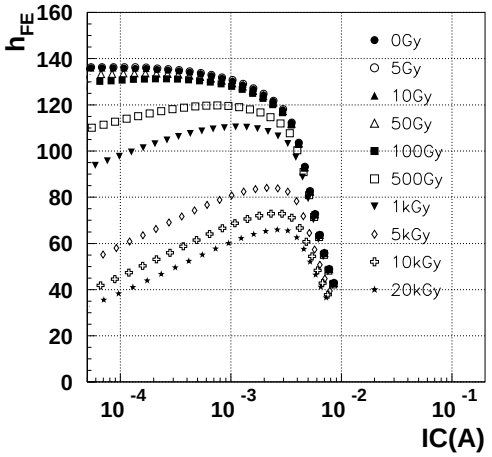

Figure 5-13 Result of gamma irradiation on a NPN transistor. The transistor was biased during the irradiation.

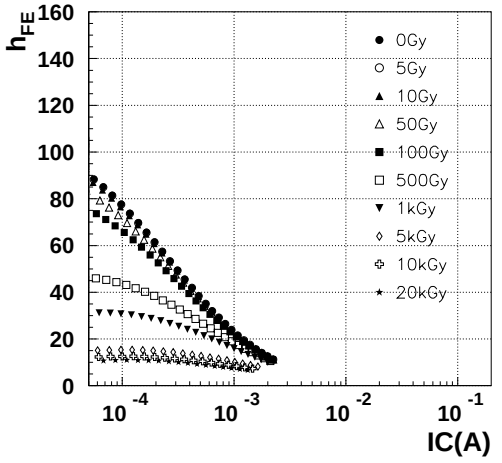

Figure 5-14 Result of gamma irradiation on a PNP transistor. The transistor was not biased during the irradiation.

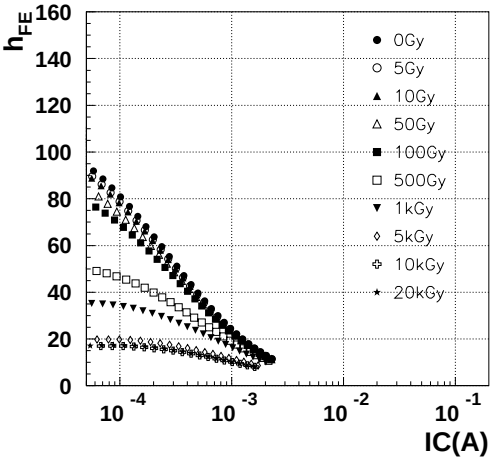

Figure 5-15 Result of gamma irradiation on a PNP transistor. The transistor was biased during the irradiation.

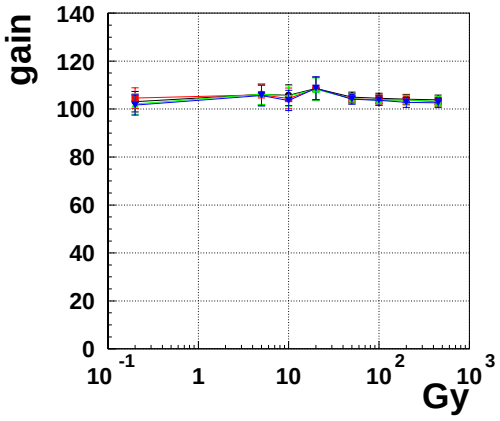

Figure 5-16 Gain of TL592B versus total gamma-ray dose.

5.2.3 Neutron irradiation (I)

5.2.3.1 Setup

The neutron irradiation tests were performed by placing ASD chips and transistor packages near the extracted proton beam line (EP1) from the 12GeV Proton Synchrotron at KEK. The test samples were contained in lead boxes, the wall thickness of which was 25mm or 40mm, to shield them from gamma radiation. In order to measure the neutron fluence, metal foils (cobalt and nickel) were also put in each box. These lead boxes were placed at various positions from the beam line, and were left irradiated for typically one to three weeks.

Some transistor samples were biased during the irradiation in the same way as in the gamma irradiation tests, while the others were unbiased (all the pins were floated). All the ASD chips were unbiased (all the pins were floated) during the irradiation.

5.2.3.2 Fluence calculation

The neutron fluence was measured using the activation method based on the reaction ^{59}Co(n,2n)^{58}Co. A calibrated germanium detector was used to measure the radioactivity of the cobalt foils after the irradiation. For neutrons of the proton beam origin, the energy spectrum is well approximated to scale as E^{-1}, where E is the neutron kinetic energy[11]. With this approximation for the neutron energy spectrum, together with the cross-section of the reaction ^{59}Co(n,2n)^{58}Co[12], the measured radioactivity of ^{58}Co could be converted to the neutron fluence. Then, following the method described in reference [13], the fluence was converted to the 1MeV equivalent neutron fluence.

As a cross-check, the reaction ^{58}Ni(n,p)^{58}Co was also used to obtain the neutron fluence. Its sensitive energy region is somewhat lower (2~20 MeV) than the one for ^{59}Co(n,2n)^{58}Co (above 10MeV). The fluence based on ^{58}Ni(n,p)^{58}Co was found to be 1.2 to 1.9 times higher than the ^{59}Co(n,2n)^{58}Co based value. Most of the difference could be attributed to the assumption of the E^{-1} proportionality for the neutron energy spectrum.

5.2.3.3 Result

Neutron irradiations on the individual transistors with or without biasing were made up to the total fluence of 2.4×10^{13} 1MeV equivalent neutrons/cm^2. Figure 5-17 to Figure 5-20 show the results of the h_{FE} measurements as a function of I_C for each of NPN/PNP transistors with/without biasing (one transistor sample for each plot). The h_{FE} values at I_C = 0.4 mA are plotted in Figure 5-21 to Figure 5-24 as a function of the neutron fluence for all the measured samples. One can clearly see from those plots that the unbiased case has larger deterioration than the biased case for both types of transistors.

We made some more measurements on the transistors without biasing. Figure 5-25 and Figure 5-26 show the h_{FE} values normalized to the ones before the irradiation as a function of I_C. Figure 5-27 and Figure 5-28 show the normalized h_{FE} values at I_C = 0.4mA as a function of the neutron fluence. After the irradiation of 1.1×10^{12} 1MeV equivalent neutrons/cm^2, the decrease of h_{FE} at the nominal value of I_C was found to be within 10%.

Gain values of the preamplifier part of the ASD chips as a function of the neutron fluence are shown in Figure 5-29. One can easily see that the gain difference after the irradiation of 1.2×10^{12} 1MeV equivalent neutrons/cm^2 is within 5%. The ENC values as a function of the input capacitance were measured as shown in Figure 5-30. Figure 5-31 shows the ENC values at a nominal value of the input capacitance (165pF) as a function of the neutron fluence. There is no apparent difference in ENC up to 1.7×10^{13} 1MeV equivalent neutrons/cm^2, which is an order of magnitude higher than that required for 10 years of LHC running.

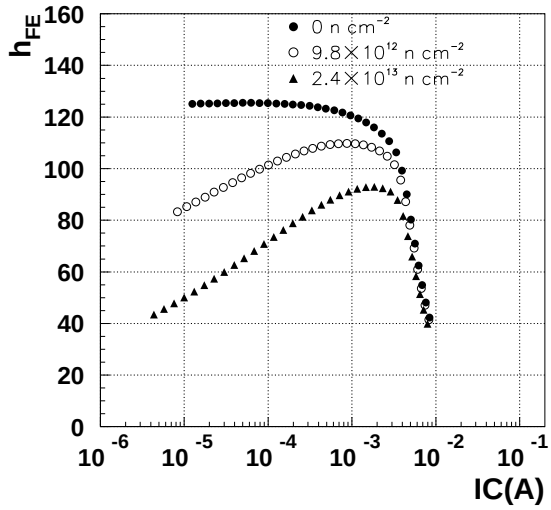

Figure 5-17 Result of neutron irradiation on NPN transistors. The transistors were not biased during the irradiation.

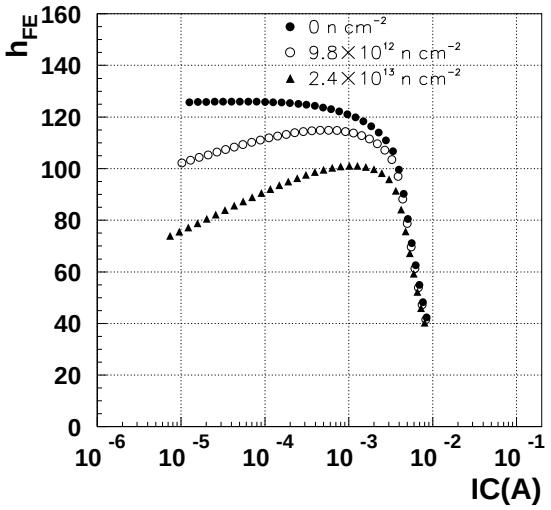

Figure 5-18 Result of neutron irradiation on NPN transistors. The transistors were biased during the irradiation.

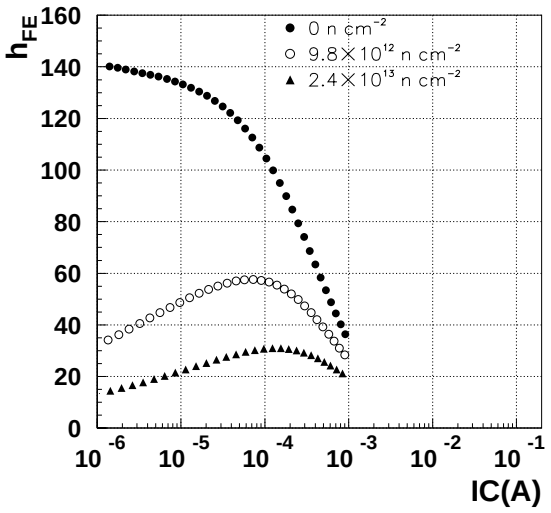

Figure 5-19 Result of neutron irradiation on PNP transistors. The transistors were not biased during the irradiation.

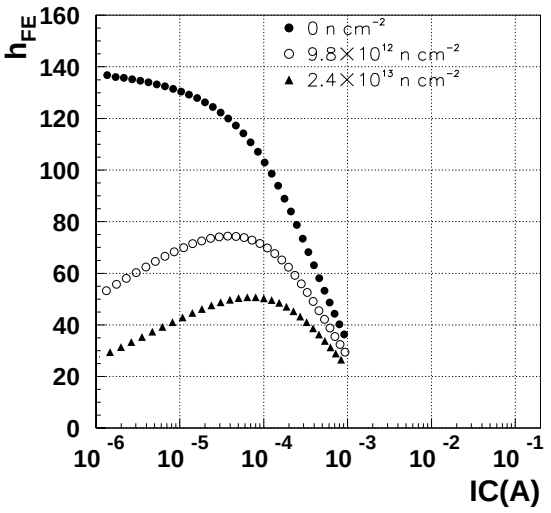

Figure 5-20 Result of neutron irradiation on PNP transistors. The transistors were biased during the irradiation.

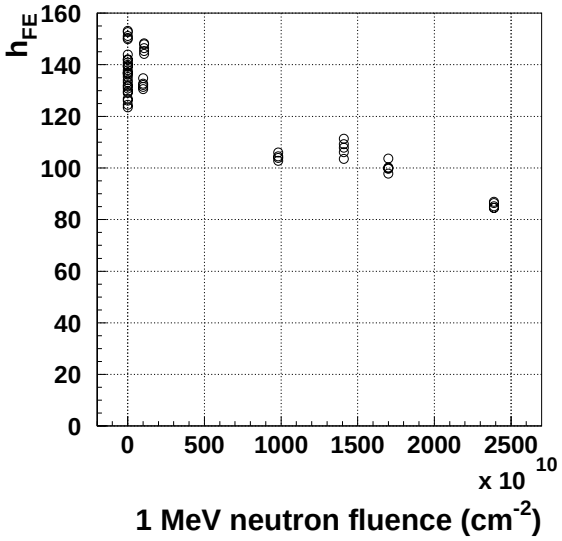

Figure 5-21 h_{FE} values at I_C = 0.4mA for NPN transistors as a function of neutron fluence. The transistors were not biased during the irradiation.

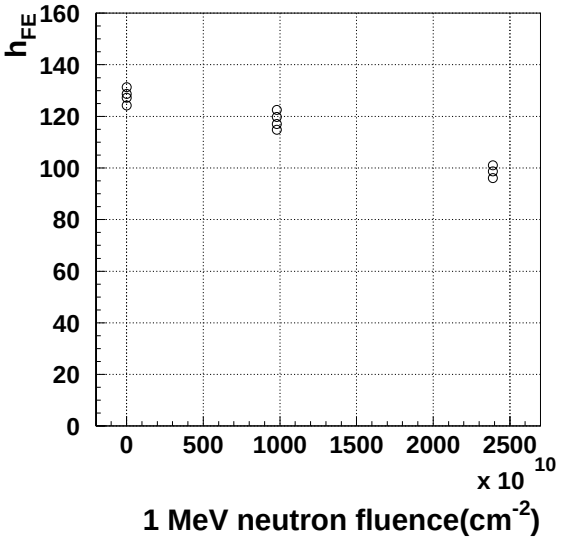

Figure 5-22 h_{FE} values at I_C = 0.4mA for NPN transistors as a function of neutron fluence. The transistors were biased during the irradiation.

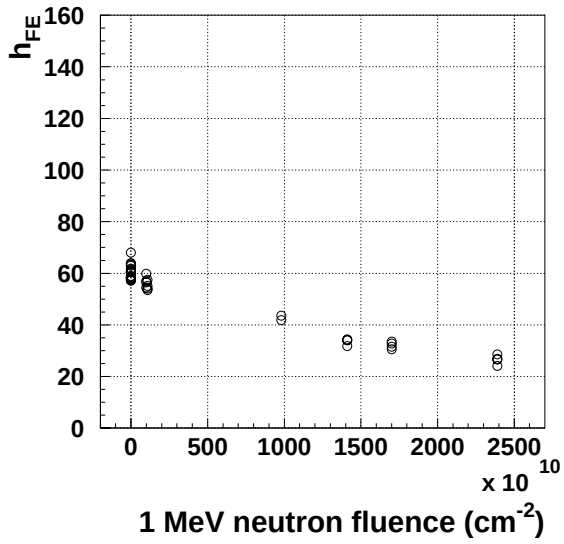

Figure 5-23 h_{FE} values at I_C = 0.4mA for PNP transistors as a function of neutron fluence. The transistors were not biased during the irradiation.

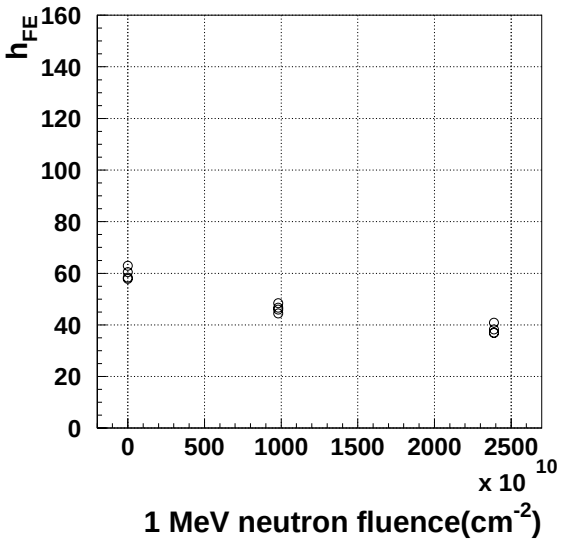

Figure 5-24 h_{FE} values at I_C = 0.4mA for PNP transistors as a function of neutron fluence. The transistors were biased during the irradiation.

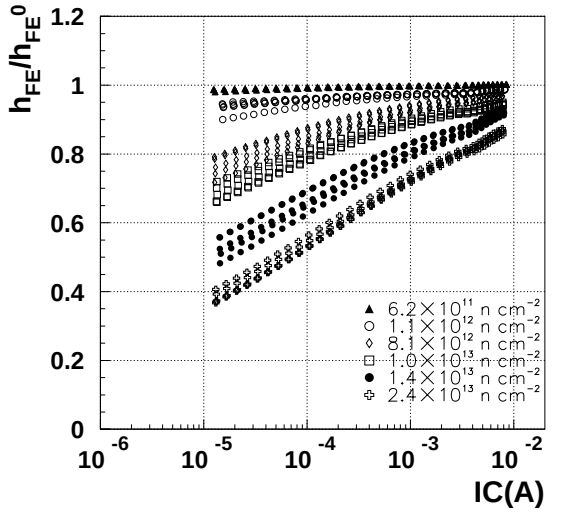

Figure 5-25 Normalized h_{FE} values as a function of I_C for NPN transistors for various neutron fluences. The transistors were not biased during the irradiation.

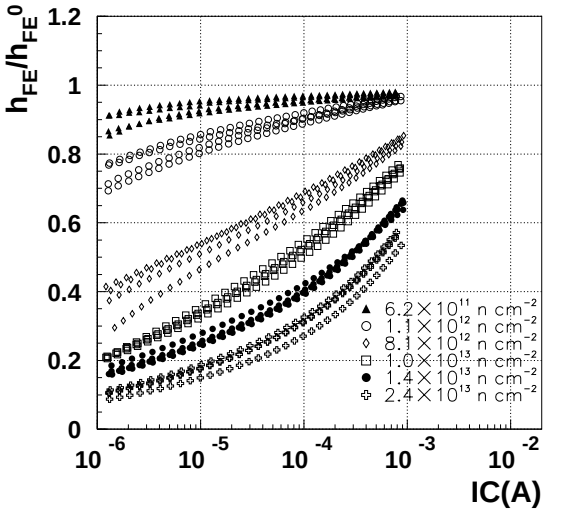

Figure 5-26 Normalized h_{FE} values as a function of I_C for PNP transistors for various neutron fluences. The transistors were not biased during the irradiation.

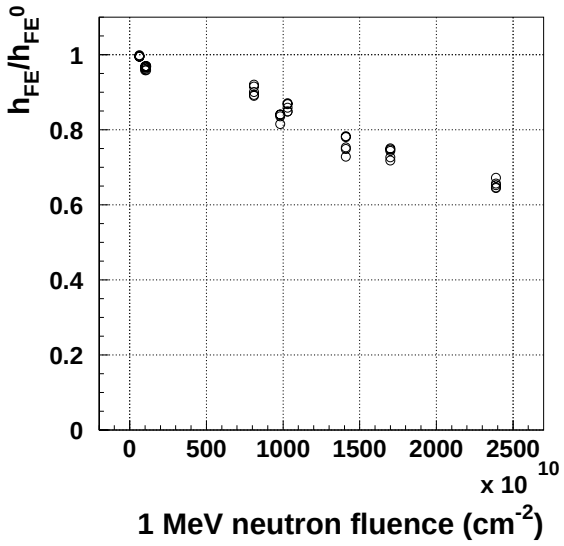

Figure 5-27 Normalized h_{FE} values at I_C = 0.4mA for NPN transistors as a function of neutron fluence. The transistors were not biased during the irradiation.

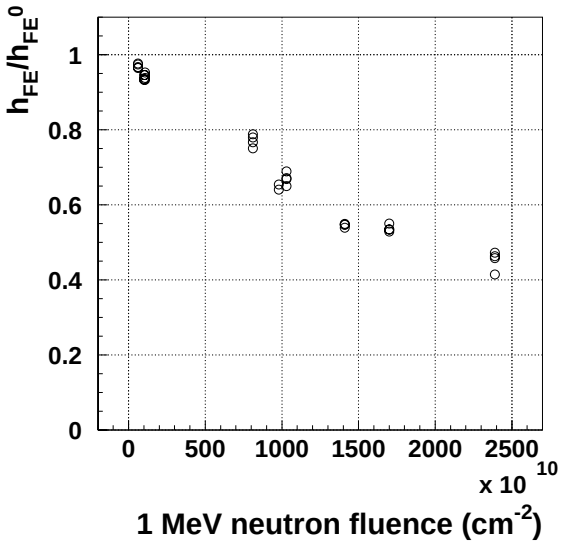

Figure 5-28 Normalized h_{FE} values at I_C = 0.4mA for PNP transistors as a function of neutron fluence. The transistors were not biased during the irradiation.

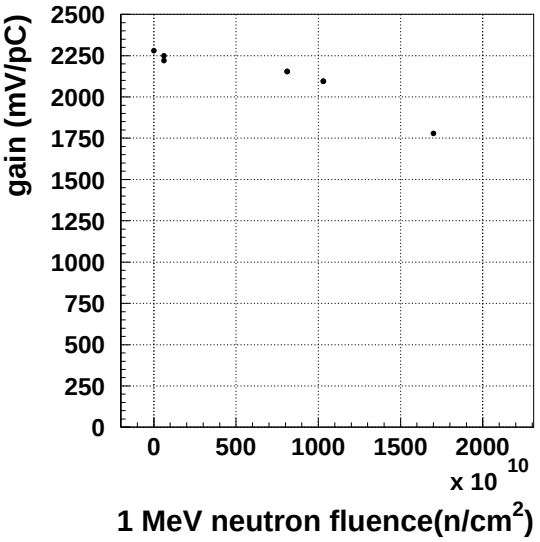

Figure 5-29 Gain values of ASD chips versus neutron fluence.

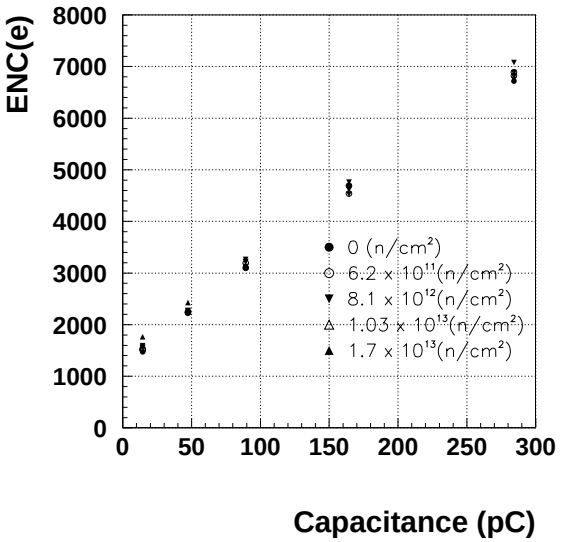

Figure 5-30 ENC values of ASD chips as a function of input capacitance for various neutron fluences.

5.2.4 Neutron irradiation (II)

5.2.4.1 Setup

Additional neutron irradiation test of the components of the ASD Board was performed using the Prospero facility in France. The neutron fluence in this facility are well measured as the neu-

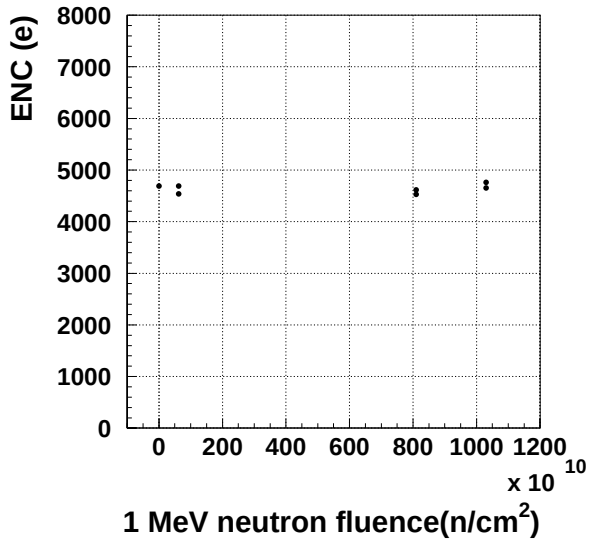

Figure 5-31 ENC values of ASD chips at the input capacitance of 165pF as a function of neutron fluence.

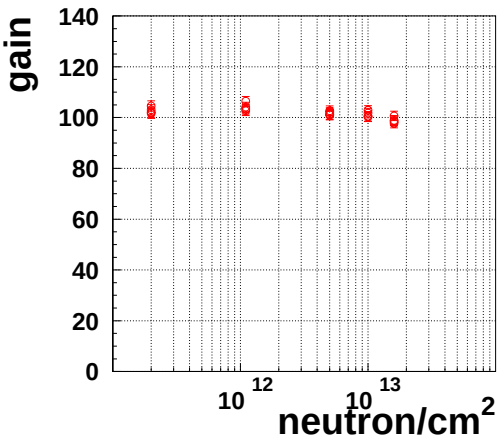

Figure 5-32 Gain of TL592B versus neutron fluence.

trons are from a reactor. The uncertainties on the fluences were smaller that those in the previous test.

We have tested the diodes and the video amplifiers (TL592B) described in Section 5.2.2. Each type was grouped into four samples where each group was irradiated at different distance from the reactor, resulting in different neutron fluence exposed. These fluences were 1.1×10^{12}, 5.0×10^{12}, 1.0×10^{13} and 1.6×10^{13} neutrons / cm^2 of 1MeV equivalent. All the samples were not biased during the irradiation. After the irradiation, their properties were measured.

5.2.4.2 Result

The V-I curves were checked in the same way for the gamma-ray test with resdpect to the biasing range. There was no significant difference for different fluence level. No products broke down after the highest neutron fluence exposed.

Figure 5-33 shows the gain of TL592B as a function of fluence. The first dots in the left of the figure show the gain before irradiation, which were measured prior to the gamma-ray test described before. A small deterioration in gain was observed at the highest fluence level, but no significant deterioration was observed at 1.1×10^{12} 1MeV equivalent neutrons / cm^2 . No change was observed in rise time neither in fall time, as expected from the gamma ray test.

The components of the ASD board including the ASD chips are expected to survive in the environment under the neutron fluence equivalent to that of 10 years of LHC running

5.2.5 Summary

As a result of the irradiation tests, it is proved that the ASD chips , their component transistors and the component devices of the ASD Board retain the properties required for the TGC readout after 10 years of LHC running even at the location of the worst background conditions in the forward muon trigger station.

There are two related remarks in order. In our tests, due to the limitations of the test facilities and time, we did not perform the irradiation test of the ASD chips with biasing. As mentioned above, however, from the comparison of biased and unbiased cases at the transistor level, the performance of the ASD chips with biasing is expected to be better than that without biasing.

For the ASD Board, we tested only component devices of the board. However the main components were checked to survive the radiation environment for ten-year running; the ASD Boards are also expected to be tolerant against the same radiation condition.

We also tested the devices for radiation tolerance at a high rate and a low rate. Lower dose-rate environments are expected to be severer for electronics devices, but the tested devices survive even a low dose-rate environment.

We have quoted the reference radiation values for the test which correspond to the worst location of TGCs in the forward muon trigger station. As for the EI station (at $z = 7$ m), the radiation level is estimated to be about an order of magnitude higher than that at the worst position of the trigger station. First of all, our test results show that the ASD chips are tolerant against such a high radiation. In addition, the ASD Boards will be mounted at the outer edge of the EI chamber, where the radiation level is approximately the same as (or even less than) that of the worst region of the trigger station. Therefore the same ASD chips can be used for the TGCs in the EI station.

6 Mass-production

6.1 ASD IC

The new masks for the mass-production, the inspection setup for the production line at SONY were produced and the criteria for the test was specified by the end of 1998. Mass-production of the 100,000 pieces of the ASD chips was done during the summer of 1999. The instruments for the inspection at SONY were limited (e.g. limited test signal sources, insufficient sampling rate of a wave form for a fast signal), but we believe that we found most (if not all) of the failed chips by simply measuring the DC characteristics. In addition to the DC characteristics, the gain of the preamplifier was measured with slower shaping. The offset voltage of the comparator was measured using a slowly ramping signal. Table 6-1 shows a list of conditions for the inspection and selection criteria. The criteria was defined taking into account both the fluctuation in the process among various production lots and the deviation in the same lot. The fluctuation of the process between production lots is much larger than the deviation within a particular lot. The h_{FE} of the transistor fluctuates from 55% to 170% and the V_{BE} by ±30mV. The resistivity fluctuation of a poly-silicon resistor is ±20%, and capacitance of a MIS capacitor is ±8%.

Since we have produced all the ASD ICs in a single lot, much less deviation in the ASD characteristics was expected. We will not make an additional inspection of the chips prior to assembly. We did a pre-mass-production (5,000 chips) in order to verify the inspection setup in 1998. Hence we have more than the required number of ASD chips, 100,000 pieces including about 10% spares for the experiment. We can place an order for the chips anytime before the process is discontinued by SONY, subject to a minimum order of 2,000 pieces. The process is expected to remain running for two years after the announcement of its discontinuance.

Table 6-1 Inspection conditions and selection criteria for the ASD chips.

	item		minimum	typical	maximum
1	DC power currents at standard voltage (±3.0V)	+3.0V	39.0mA	42.5mA	47.5mA
		–3.0V	–13.5mA	–16.0mA	–19.0mA
2	DC power currents at ±2.7V (ratio to those at ±3.0V)	+2.7V	80%	82%	84%
		–2.7V	84%	86%	88%
3	DC power currents at ±3.3V (ratio to those at ±3.0V)	+3.3V	116%	118%	120%
		-3.3V	112%	114%	116%
4	Input bias current of V_{th}		0µA		2µA
5	Output voltages at preamplifier analog outputs		0.59V	0.76V	0.82V
6	LVDS output voltages and their differential voltages at V_{th} = ±100mV	logic-H	1.35V	1.47V	1.60V
		logic-L	0.89V	1.05V	1.14V
		differential	0.33V	0.42V	0.52V
7	Offset voltages of comparators		-21mV	0 mV	21mV
8	Gain of the preamplifier (ratio to a calibration standard)		65%	100%	140%

6.2 ASD Board

The sheet layout that contains six 16-ch ASD Boards was designed. The size of the sheet was optimized to minimize the cost of both PC boards and assembling. The tool to electrically inspect the PC board was also developed. The tool, which has a bed of pins as probes, checked connection and no-shorting between lands on the PC board. The mass-production and inspection of the PC boards was completed in August 1999 and ready for assembling.

The assembling procedure is the following.

1. print cream solder on the sheet of the PC board.
2. mount all the SMD components on the sheet.
3. re-flow soldering.

1. through 3. will be done automatically by a SMD assembling robots.

4. Inspection on soldered pads is done by a computer analyzing the image of the boards taken with laser light.
5. Connectors are hand-mounted and soldered using a flow-soldering bath.
6. Apply a heat cycle (4 cycles from 0 to 70 ˚C in 24 hours)
7. Six 16-ch ASD Boards are separated from the sheet and packaged.

200 ASD Boards were assembled in May 1999 in order to verify the production procedure for the mass-production. No ASD Board failure was found after through the production procedure.

The total number of the ASD Boards to be produced is 23,000 boards, including about 10 % spares.

6.3 Inspection

All the assembled ASD Boards will be inspected prior to the shipping to the chamber production sites. We developed an inspection system that consists of a test pulse generator and a VME hit-latch module, as shown in Figure 6-1. Up to four ASD Boards to be tested are mounted on the test pulse generator board, which provides simulated TGC signal (charge impulse with variable amplitude) to proper input pins of the ASD Boards. The hit-latch module provides DC power, threshold voltage (variable) and test pulse (fixed amplitude, ±0.09 pC) to the ASD Boards, and receives LVDS hit signals from the ASD Boards. The hit signals are latched on the register of the module when they coincide with a gate signal (variable gate width). The data on the register are read via the VME bus. All the variable parameters, including the timing, of the trigger and gate signals can be set via a computer.

Since all ASD ICs have been tested in the production line of SONY as mentioned in section 6.1, any failures of the ASD Boards would come from failure of the soldering. The inspection procedure of the ASD Board is decided as following.

1. check the gain of the ASD Board.

   Test pulses having -0.02 pC charge are sent from the test pulse generator board and the register that has latched hit signals are read while varying the threshold voltage.

2. simulate the normal operation.

   Test pulses having -0.2 pC charge are sent from the test pulse generator board and the register that has latched hit signals are read with the threshold voltage fixed at -100 mV (~ 9 fC).

3. check the test pulse function from the hit-latch module.

   Test pulses of -0.09 pC charge are sent from the hit-latch module and the register that has latched hit signals are read with the threshold voltage fixed at -100 mV (~ 9 fC).

Failed boards will be repaired and retested. From our experience in mass-productions, the failure rate before any test is estimated to be less than 1 %.

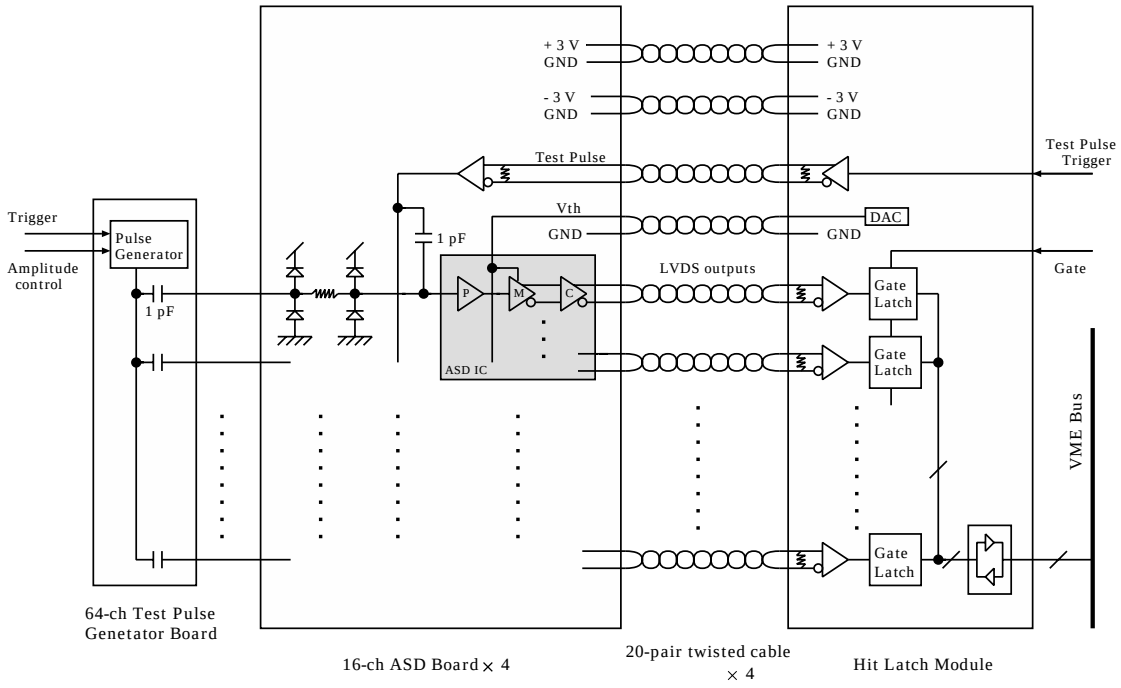

Figure 6-1 The ASD Board inspection system.

7 Schedule

The mass-production of the TGC chamber has started in spring 1999. 100,000 chips of the ASD ICs was delivered to KEK in October 1999. The other parts will be delivered by the end of 1999. The pre-mass-production of ASD Boards was completed by May 1999 in order to check the production procedure. We plan to start the mass-production of ASD Boards by January 2000 and plan to complete by the end of March 2000. Inspection on the ASD Boards will be completed by the first quarter of 2001 in time for mounting to the TGCs.

Appendix

The detailed schematics (Figure 1a and Figure 1b), the PC board layout (Figure 2) , the parts list (Table 1) and the connector pin assignments (Table 2) are shown below.

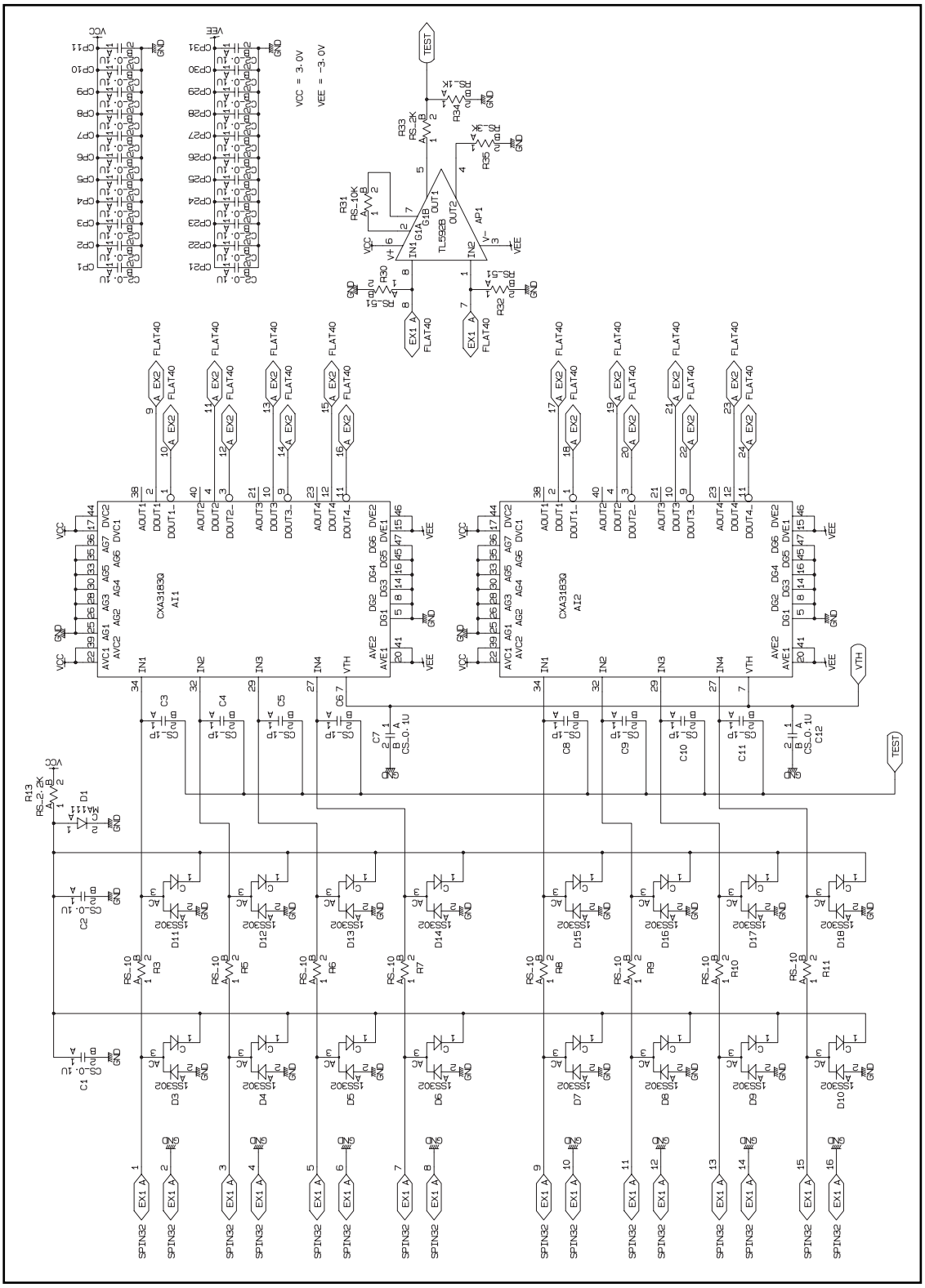

Figure A-1a Schematics of the ASD Board, part-1/2

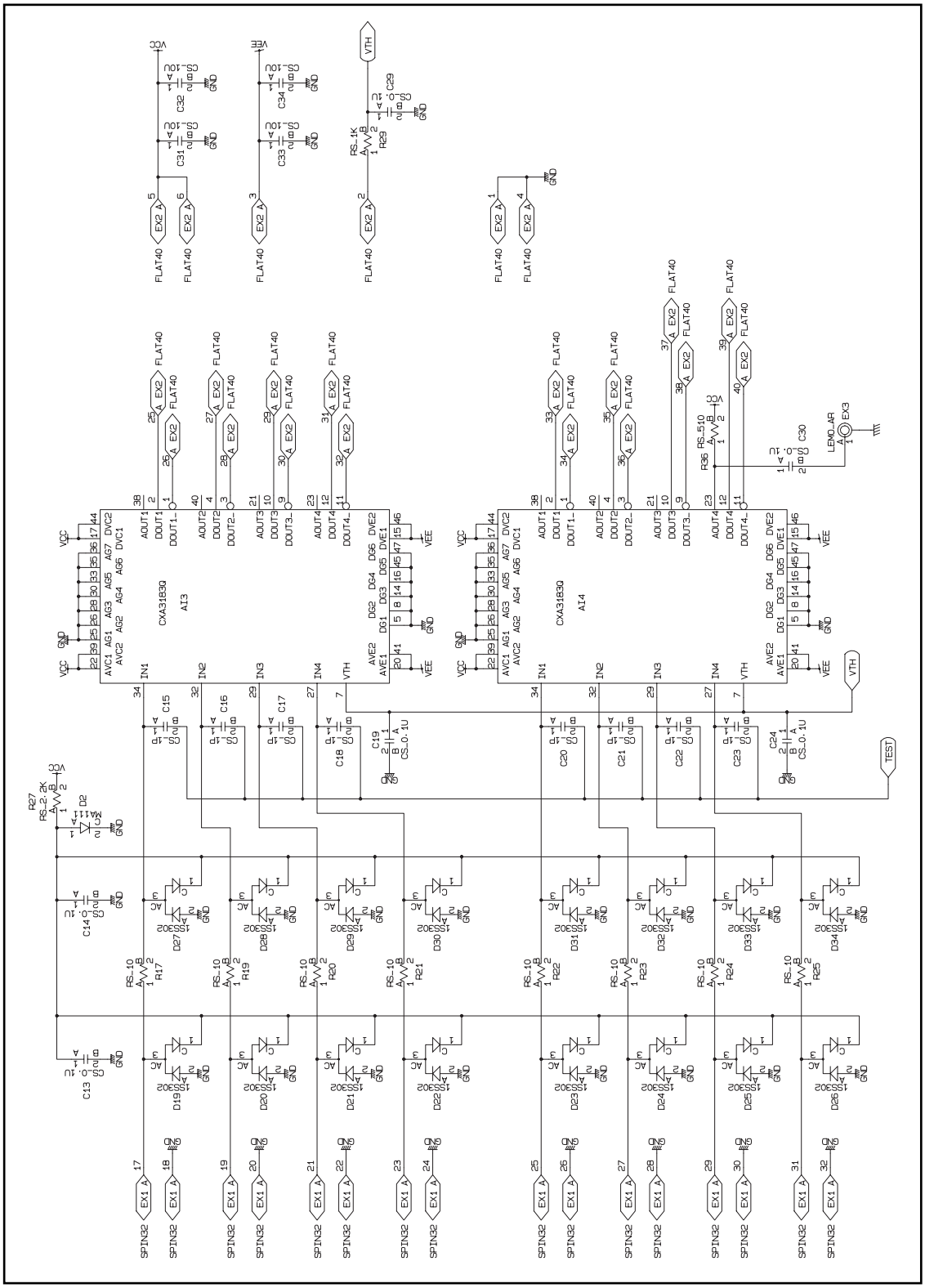

Figure A-1b Schematics of the ASD Board, part-2/2

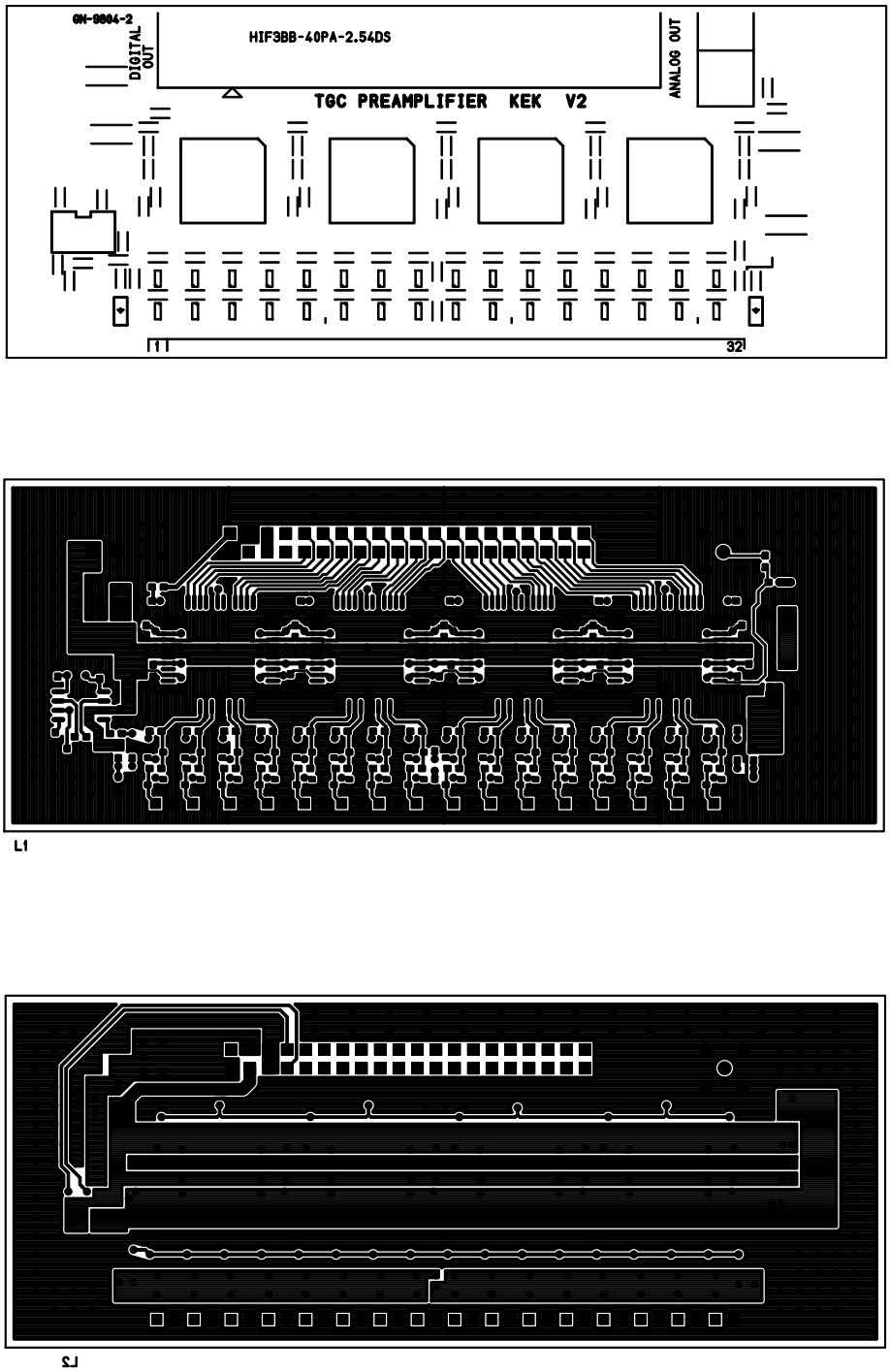

Figure A-2 Layout of the ASD Board.

Table A-1 Parts list.

No.	name	type	No. of pieces
1	ASD IC	CXA3183Q (SONY)	4
2	Video Amplifier IC	TL592B (TI)	1
3	input	399-10-132-10-009 (PRECI-DIP)	1
4	output connector	Flat 40 right-angle (HONDA)	1
5	analog output	LEMO type right-angle	1
6	diode	1SS302 (Toshiba)	32
7	diode	MA111 (Panasonic)	2
8	capacitor	ceramic 1pF	16
9	capacitor	ceramic 0.1 µF	32
10	capacitor	ceramic 10 µF	4
11	resistor	10 Ω	16
12	resistor	51 Ω	2
13	resistor	510 Ω	1
14	resistor	1 kΩ	1
15	resistor	2 kΩ	1
16	resistor	2.2 kΩ	2
17	resistor	3 kΩ	1
18	resistor	10 kΩ	1

Table A-2 Pin assignment.

pin No.	name	name	pin No.
1	GND	Vth	2
3	-3.0 V	GND	4
5	+3.0 V	+3.0 V	6
7	test pulse	$\overline{\text{test pulse}}$	8
9	hit 0	$\overline{\text{hit 0}}$	10
11	hit 1	$\overline{\text{hit 1}}$	12
13	hit 2	$\overline{\text{hit 2}}$	14
15	hit 3	$\overline{\text{hit 3}}$	16
17	hit 4	$\overline{\text{hit 4}}$	18
19	hit 5	$\overline{\text{hit 5}}$	20
21	hit 6	$\overline{\text{hit 6}}$	22
23	hit 7	$\overline{\text{hit 7}}$	24
25	hit 8	$\overline{\text{hit 8}}$	26
27	hit 9	$\overline{\text{hit 9}}$	28
29	hit 10	$\overline{\text{hit 10}}$	30
31	hit 11	$\overline{\text{hit 11}}$	32
33	hit 12	$\overline{\text{hit 12}}$	34
35	hit 13	$\overline{\text{hit 13}}$	36
37	hit 14	$\overline{\text{hit 14}}$	38
39	hit 15	$\overline{\text{hit 15}}$	40

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